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Digital Control Bridge/Bridgeless PFC Converters with Modified Current Controller for ZCD Reduction

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***Abstract*— The power factor correction (PFC) converters built for telecom applications must meet certain standards in order to keep the total harmonics distortion (THD) at the specified low levels to reduce the current stresses, reduce the power losses and hence increase the converter efficiency and input power factor (PF). Thus, in this paper, the small-signal stability models of the telecom bridge and bridgeless PFC converters are derived and based on the derived stability models, the fast-dynamic response integral-proportional (IP) current control technique is proposed to improve the control loops performance around the current waveform zero-crossing point, reduce zero crossing distortion (ZCD), reduce the THD, and reaches the input current PF near to unity. The digital simulation modeling using PSIM software of the 2.5 kW bridge and bridgeless PFC converters is performed to show the converter's performance with the proposed current technique as compared with the conventional proportional-integral (PI) control technique. The proposed current controller in this work improves the current control loop performance, reduces the ZCD period, reduces the THD to about 5% and reaching converters input PF near unity in both bridge and bridgeless PFC converters.**

Keywords*— *telecom PFC, ZCD, THD, PI&IP Controllers, small signal models, PSIM modeling.

I. INTRODUCTION

With the industrial development and the spread of control and communication systems using 5G telecom systems, the need of supplying the DC power with the high density, high conversion efficiency, and high PF increased the modifications that occur in the conventional AC-DC power supplies by proposing new techniques and implement new topologies to enhance the circuit performance and operational requirements. For the 5G telecom power applications, the two-stage AC-DC power supplies shown in Fig. 1 are the best choice to be implemented for supplying electrical power with high efficiency and high PF [1,2]. The two-stage power supply for telecom servers consists of a PFC stage to improve the supply PF and a DC-DC converter stage to increase conversion efficiency and maintain the appropriate output voltage regulation [3,4].

Many PFC circuit topologies are used for the telecom front stage, including bridge, bridgeless, and interleaved PFC converters [2-4]. Typically, the implementation of telecom PFC converters in these PFC topologies is based on the operation principle of the boost converter to adjust the phase difference between the supply voltage and current waveforms and thus control the input supply PF.

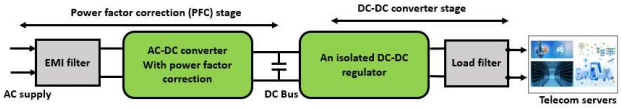

Fig. 1. Structure of the two-stage power supply in industrial applications

In PFC boost converters, the proportional-integral (PI) controllers are utilized as a basic approach in the current and voltage control loops and can be implemented inside the DSP MCU. However, the MCU's analog-to-digital conversion (ADC) process and the PI controllers' slow dynamic response in control loops, particularly at the AC current zero crossing point introduce a dead period in the supply current waveform known as zero-crossing distortion (ZCD) period [5,6]. When ZCD occurs, the THD level rises, conduction losses increase, conversion efficiency decreases, and the input supply power factor (PF) decreases [7,8].

Many control schemes are previously recommended to minimize current distortion in digital control PFC converters with conventional PI controllers, such as modifying the feedback current signal for the inner current-control loops using digital current filters to reduce current error and therefore current distortion [9]. Also, Variable on-time (VOT) switching control schemes using model predictive control approaches to optimize the precise dead time surrounding zero crossing distortion and then modify the converter duty cycle to minimize this dead time. [10-11].

When compared to the conventional PI controller, The integral-proportional (IP) controller offers a faster dynamic response and less overshoot than the typical PI controller. The IP controller has two current control loops, not just one like the PI controller, where the integral gain feeds in front and the proportional gain feeds backward, allowing for a reliable and sufficient inductor current track to the reference current, reducing ZCD, THD, and providing a converter with a high PF.

In this paper, the optimal design of the PFC converter's current control loops is proposed to reduce ZCD. The designed control systems stability is checked using the bode diagram and root locus, the PSIM modeling of the bridge and bridgeless PFC converters is performed to check the performance of the PFC converters with the designed control techniques under different loading conditions and to investigate the reliability of the proposed control technique to reduce the current ZCD as compared with the conventional one in both PFC topologies.

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II. SMALL-SIGNAL STABILITY OF THE PFC CONVERTERS

A. Bridge PFC boost converter

Figure 2 shows the complete structure of the digital control bridge PFC boost converter stage implemented for the two-stage industrial power supply. The operation principle of the classical bridge PFC boost converter is based on the operation of the single-phase boost converter.

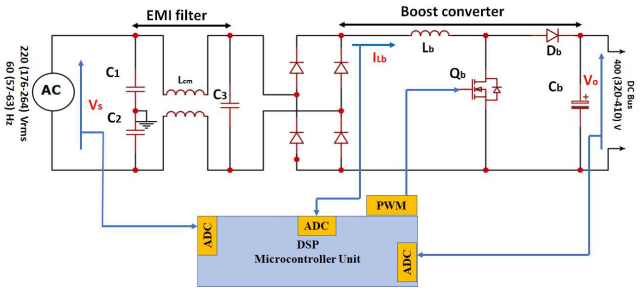

Fig. 2. Configuration of digital control bridge PFC converter topology

The change in the inductor current (I_{Lb}) and the DC bus voltage (V_o) can be represented as follows assuming the single-phase boost converter unit is operating in the continuous current conduction (CCM) mode.

$$\frac{dI_{Lb}}{dt} = \frac{V_{in}}{L_b} - \frac{V_o(1-D)}{L_b} \quad (1)$$

$$\frac{dV_o}{dt} = -\frac{V_o}{R\,C_b} + \frac{I_{Lb}(1-D)}{C_b} \quad (2)$$

where, D is the duty cycle, R is the load value in Ω.

Assume that at the selected operational point $(i_{Lb}, v_{in}, v_o, and\ d)$, all variables $(I_{Lb}, V_{in}, V_o, and\ D)$ are at the steady state and the small-signal AC variation are $(i^*_{Lb}, v^*_{in}, v^*_o, and\ d^*)$, where

$$I_{Lb} = i_{Lb} + i^*_{Lb}\ ;\ V_{in} = v_{in} + v^*_{in}\ ;\ V_o = v_o + v^*_o\ ;\ D = d + d^* \quad (3)$$

To control the output DC voltage (V_o) and inductor current (I_{Lb}), the planned control system must adjust the converter operating duty cycle (D) based on the small-signal variation.

by inserting (3) into (1) and (2). And, using the averaging model, which presumes that the capacitor voltage changes and the inductor current change is zero over the switching period in the steady-state [2], equations (4) and (5) can be obtained.

$$\frac{d(i^*_{Lb})}{dt} = \frac{1}{L_b}(v^*_{in}) + \frac{v_o}{L_b}(d^*) - \frac{(1-d)}{L_b}(v^*_o) \quad (4)$$

$$\frac{d(v^*_o)}{dt} = \frac{(1-d)}{C_b}(i^*_{Lb}) + \frac{i_{Lb}}{C_b}(d^*) - \frac{1}{R\,C_b}(v^*_o) \quad (5)$$

The bridge CCM PFC converter's small signal stability model is presented in state space matrix form as follows

$$\begin{bmatrix} i^*_{Lb} \\ v^*_o \end{bmatrix} = \begin{bmatrix} 0 & -(\frac{1-d}{L_b}) \\ (\frac{1-d}{C_b}) & \frac{-1}{R\,C_b} \end{bmatrix} \begin{bmatrix} i^*_{Lb} \\ v^*_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L_b} & \frac{V_o}{L_b} \\ 0 & \frac{i_{Lb}}{C_b} \end{bmatrix} \begin{bmatrix} v^*_{in} \\ d^* \end{bmatrix} \quad (6)$$

B. Bridgeless PFC boost converter

Figure 3 illustrates the complete structure of the digital control bridgeless PFC converter topology. In this topology, the storage energy element represented by the boost inductor L_b can be used as a single unit or divided into two units L_{b1}, L_{b2} to improve the thermal performance and to prevent high dv/dt transients from being applied directly to the input terminal. In the analysis, we assume that the bridgeless boost converter employed in this work is working in CCM mode, and the operation of the bridgeless PFC for the positive AC cycle and negative AC cycle is symmetrical.

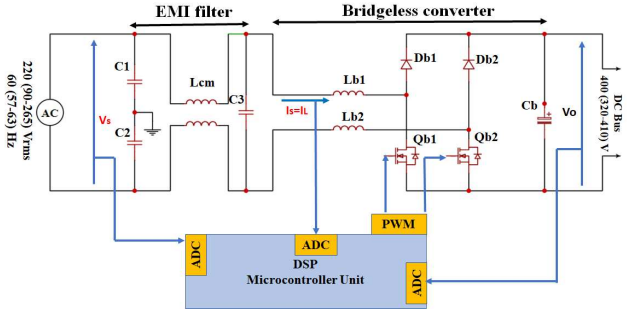

Fig. 3. Configuration of digital control bridgeless PFC converter topology

The change in the supply current which equal to the inductor current (I_s=I_{Lb}) and the DC bus voltage (V_o) in the bridgeless PFC boost converter can be mathematically described as:

$$\frac{dI_{Lb}(t)}{dt} = \frac{V_s - V_o(1-D)}{Lb_1 + Lb_2} \quad (7)$$

$$\frac{dV_o(t)}{dt} = \frac{I_{Lb}(1-D)}{C_b} - \frac{V_o}{R\,C_b} \quad (8)$$

The small-signal stability model for the bridgeless CCM PFC converter is represented in matrix form using the same technique as the average small-signal modeling used in the bridge topology:

$$\begin{bmatrix} i^*_{Lb} \\ v^*_o \end{bmatrix} = \begin{bmatrix} 0 & -(\frac{1-d}{L_b}) \\ (\frac{1-d}{C_b}) & \frac{-1}{R\,C_b} \end{bmatrix} \begin{bmatrix} i^*_{Lb} \\ v^*_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L_b} & \frac{V_s}{(1-d)L_b} \\ 0 & \frac{V_s}{(1-d)RC_b} \end{bmatrix} \begin{bmatrix} v^*_s \\ d^* \end{bmatrix} \quad (9)$$

Table I shows the specifications of the PFC converters employed in this work.

TABLE I. THE TARGET PFC CONVERTERS DESIGN SPECIFICATIONS

Design Specifications		
Parameter	***Value***	***Unit***
Supply voltage (V_s)	220 (90–265)	V
Supply Frequency (F)	60 (57–63)	Hz
DC bus Voltage (V_o)	400 (320–410)	V
Output Power (P_o)	2.5	kW
Switching Frequency (F_{sw})	100	kHz

III. CONTROL CIRCUITS DESIGN OF THE PFC CONVERTERS

A. With the conventional PI controllers

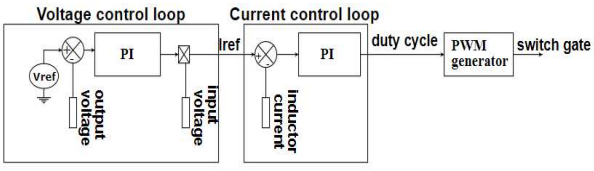

Fig. 4. Structure of the PFC boost converters conventional control circuit

As depicted in Fig. 4, the control circuit of the PFC boost converter is typically implemented inside the DSP MCU with two PI control loops. One to maintains the DC bus voltage level to the desired value (V_{ref}), and the other allows the inductor current to track the reference current (I_{ref}) generated

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by the outer voltage control loop to reduce inductor current distortion and offer input supply current with high PF.

a) Bridge PFC boost converter

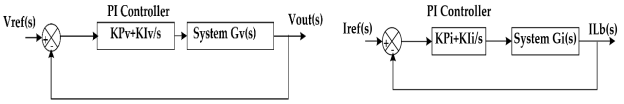
For the bridge PFC topology, the open loop TF of both control loops can be get using the small signal stability model derived in (6) as follow

$$G_v(s) = \frac{v_o^*(s)}{i_{Lb}^*(s)} \cong \frac{V_{in}}{2\,V_o\,C_b s} \tag{10}$$

$$G_i(s) = \frac{i_{Lb}^*(s)}{d^*(s)} = \frac{\frac{V_o}{L_b}s + \frac{2V_o}{L_b R C_b}}{s^2 + \frac{1}{C_b R}s + \frac{1}{L_b C_b}(1-d)^2} \tag{11}$$

At high frequency analysis (F_{sw}=100 kHz), the DC bus capacitor can be shorted, and TF $G_i(s)$ can be simplified as

$$G_i(s) \cong \frac{V_o}{sL_b} \tag{12}$$



(a) (b)

Fig. 5. PFC closed loop control systems: (a) voltage loop; (b) current loop

Block diagrams in Fig. 5 depicts the closed loops of the both control systems, where the voltage and current loop's TF can be calculated as

$$G_{CLv}(s) = \frac{V_{out}(s)}{V_{ref}(s)} = \frac{\frac{V_{in}}{2\,V_o\,C_b}.(K_{Pv}\,s + K_{Iv})}{s^2 + \frac{V_{in}\,K_{Pv}}{2\,V_o\,C_b}s + \frac{V_{in}\,K_{Iv}}{2\,V_o\,C_b}} \tag{13}$$

$$G_{CLi}(s) = \frac{I_{Lb}(s)}{I_{ref}(s)} = \frac{\frac{V_o}{L_b}.(K_{Pi}\,s + K_{Ii})}{s^2 + \frac{V_o\,K_{Pi}}{L_b}s + \frac{V_o\,K_{Ii}}{L_b}} \tag{14}$$

The transfer functions of both control loops of the bridge PFC converter can be represented by second-order systems as shown in (13) and (14), and thus the PI controller gains can be selected using these equations and the standard form of the second-order system TF by choosing a particular system bandwidth (W_n) and the undamped natural frequency (ξ) to ensure system stability in both control loops.

To minimize harmonics of the DC bus reflected by the AC input voltage at line frequency 60 Hz, the bandwidth of the outer voltage control loop must typically be very small. Furthermore, in order to track changes in the inductor current signal, the inner current-control loop needed a bandwidth wider than the outer voltage loop bandwidth. Moreover, to eliminate noise at the switching frequency (F_{sw}), The bandwidth of the current-control loop must be less than the switching frequency (Fsw) [2,5].

Therefore, for the voltage and current control loops in this work, the bandwidth Wn was considered to be about 110 rad/s and 5000 rad/s, respectively, and the undamped natural frequency was about 0.707. The PI parameters were chosen to work with a lowest range of V_o of 320 V and a rated supply voltage (V_s) of 220 Vrms for dependable operation of a controller with a wide loading range. The boost inductor L_b value is about 600 uH which is calculated based on the 20% inductor ripple current and the output bulk capacitor C_b is about 1200 uF which is calculated based on the 5% output voltage ripple as given in [2], with using these design specifications, the PI controllers parameters can be calculated for both control loops as depicted in Fig. 6.

As illustrated in the bode plot diagram in Fig. 6, the designed voltage control loop has unity gain for frequencies less than 35 Hz, therefore, represents a low-pass filter to eliminate voltage ripple at the supply frequency. Also, the developed inner current control system delivers unity gain for frequencies less than 1640 Hz, to remove switching frequency noise, it acts as a low-pass filter.

Figure 7 displays the root locus for the designed voltage and current control systems, which indicates that the control system eigenvalues are on the left-hand side of the pole-zero plane, showing that the designed control systems are fundamentally stable.

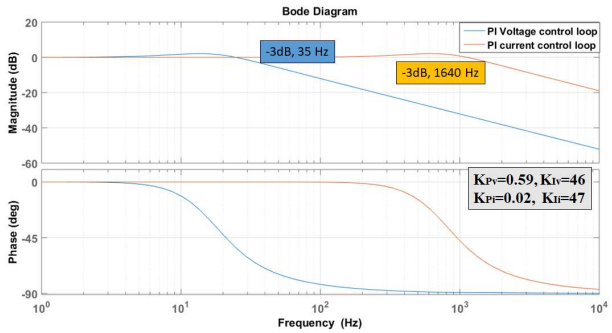
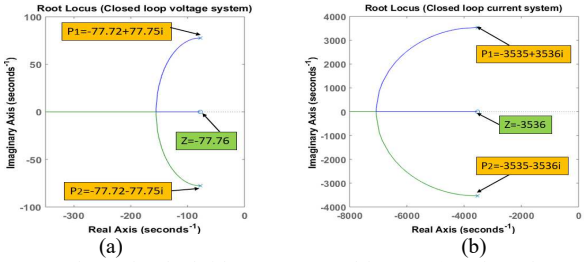


Fig. 6. Bode diagram for bridge PFC voltage and current control systems



(a) (b)

Fig. 7. Root locus for the bridge PFC control loops: (a) Voltage loop; (b) current loop

b) Bridgeless PFC boost converter

Using the derived small signal model in (9), the TF of the voltage and current systems for the bridgeless PFC topology can be obtained as given

$$G_v(s) = \frac{v_o^*(s)}{i_{Lb}^*(s)} \cong \frac{|v_s|}{2\,V_o\,C_b s} \tag{15}$$

$$G_i(s) = \frac{i_{Lb}^*(s)}{d^*(s)} = \frac{\left(\frac{V_o}{Lb\,C_b R}\right).(sRC_b + 2)}{s^2 + \frac{1}{C_b R}s + \frac{2}{Lb\,C_b}(1-d)^2} \tag{16}$$

where the $|v_s|$ is the magnitude value of the supply voltage.

The voltage control system design is the same in the bridge and the bridgeless PFC boost converters with using the PI controller, but for the bridgeless PFC converter and due to the absence of the bridge rectifier, the bandwidth of the inner current control loop is selected at about 15000 rad/s to give more reliability to the AC inductor current to track the reference current.

The controller gives unity gain for frequencies below 4900 Hz, as seen in Fig. 8, which also works as a low pass

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filter, reduces switching frequency noise. Furthermore, the designed current control system is inherently stable as observed from the root locus for the closed loop TF of the bridgeless PFC boost converter's inner current control system is depicted in Fig. 9.

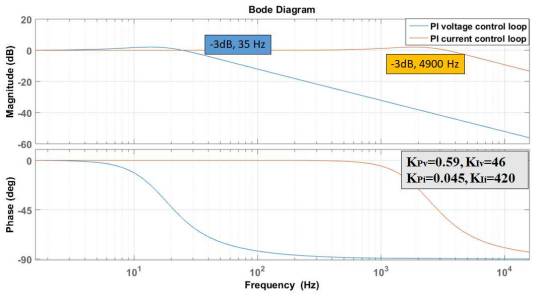


Fig. 8. Bode plot for the bridgeless PFC voltage and current control systems

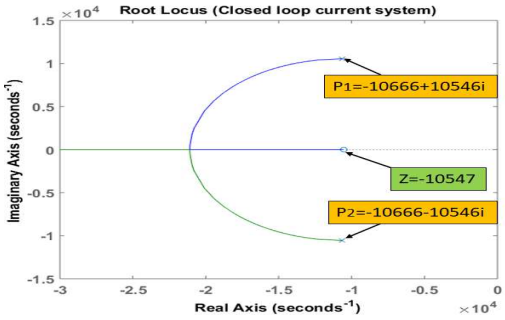


Fig. 9. Root locus for the bridgeless PFC current control system

B. With the proposed IP current controller

As compared to PI controller, the IP controller has a faster dynamic response and lower overshoot. For the dynamic performance improvement of the inner current controller and to remove the current distorting surrounding the zero-crossing point, an optimized IP controller is designed in this section to replace the PI in the bridge and bridgeless PFC boost converters' inner current-control loops.

Figure 10 depicts the proposed digital control circuit implemented inside the DSP MCU for the bridge PFC converter. The voltage control loop is still controlled with the PI controller but the current control loop is implemented using the proposed IP controller with the block diagram depicted in Fig. 11. Which it can be observe that instead of the one control loop employed by the PI controller, the IP controller uses two, where K_I gain feeds in front and the K_P gain feeds backward.

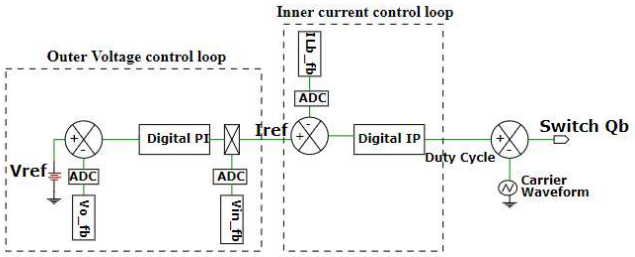


Fig. 10. Proposed digital control circuit for the bridge PFC topology

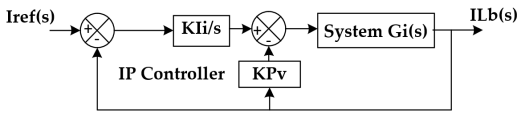


Fig. 11. Current controller implemantation using proposed IP controller

Using block diagram in Fig. 11, Equ. (17) can be derived.

$$I_{Lb} = \left[\left(I_{ref} - I_{Lb}\right)\frac{K_{Ii}}{s} - I_{Lb}K_{Pi}\right]\left[\frac{V_o}{Lb\,s}\right] \tag{17}$$

After rearranging (17), we obtain

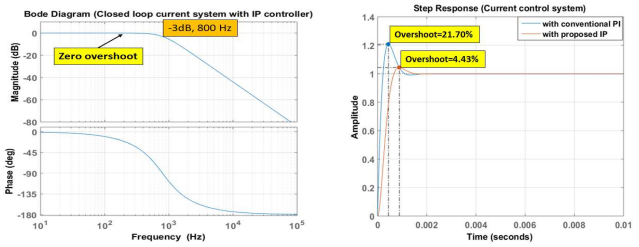
$$I_{Lb}\left[\frac{V_o}{Lb\,s}\left(\frac{K_{Ii}}{s} + K_{Pi}\right) + 1\right] = I_{ref}\left(\frac{V_o\,K_{Ii}}{Lb\,s^2}\right) \tag{18}$$

Thus, with the IP controller, the closed-loop TF of the bridge PFC current-control loop can be expressed as

$$G_{CL}(s) = \frac{I_{Lb}(s)}{I_{ref}(s)} = \frac{V_o K_{Ii}}{s^2 Lb + V_o\,K_{Pi}\,s + V_o K_{Ii}} \tag{19}$$

The fast-dynamic response IP controller can fix the inductor current's poor response to follow the reference current. This controller structure, which has two feedback control for the current control system, not simply the one utilized in the PI controller, could track the inductor current reliably and exactly to the reference current. Furthermore, unlike the TF in (14) with the PI controller, the TF with the IP controller does not have a zero, as shown in (19), resulting in a system response with less overshoot.

The IP controller settings are derived using the identical operating circumstances utilized in the PI controller. The performance of the closed-loop TF of the current control loop for the bridge PFC converter using the proposed IP current controller is shown in Fig. 12, which shows that the response has zero overshoot and that the current controller has unity gain for frequencies less than 800 Hz. Also, it is noticed that with using the IP controller instead of the PI controller, the system overshoot due to step response is reduced from 21.70% to about 4.43%.



(a) (b)

Fig. 12. Bridge PFC current control system performance with IP controller: (a) bode plot; (b) step response

Figure 13 shows the proposed digital control circuit implemented inside the DSP MCU for the bridgeless PFC topology, the voltage control loops is still controlled with the PI controller but the current control loop is implemented using two digital IP controllers which individually control the inductor currents in the positive and negative half cycles of the input supply current.

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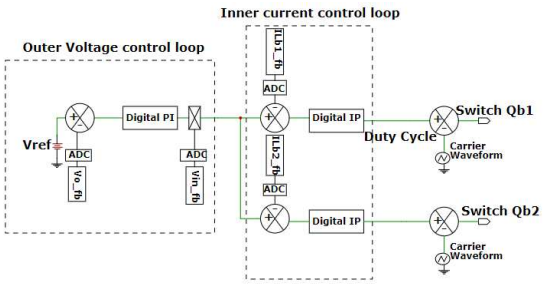
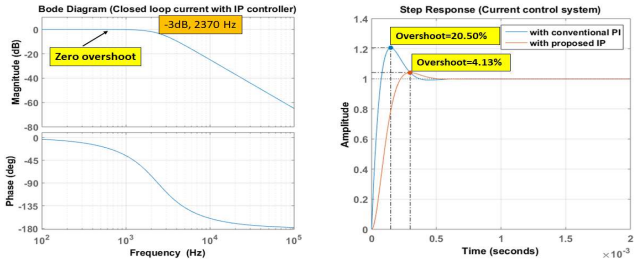


Fig. 13. Proposed digital control circuit for the bridgeless PFC topology

The proposed IP current controller replaces the PI controller in the bridgeless PFC boost converter's inner current control loops using the same design procedure. Figure 14 depicts the current control loop system performance of the bridgeless PFC boost converter, indicating that the response has zero overshoot and that the current controller provides unity gain for frequencies less than 2370 Hz. By acting as a low pass filter, this current control system helps to eliminate switching frequency noise. Also, when the IP controller is replaced the PI controller, the system overshoot with step response is reduced from 20.50% to about 4.13%.



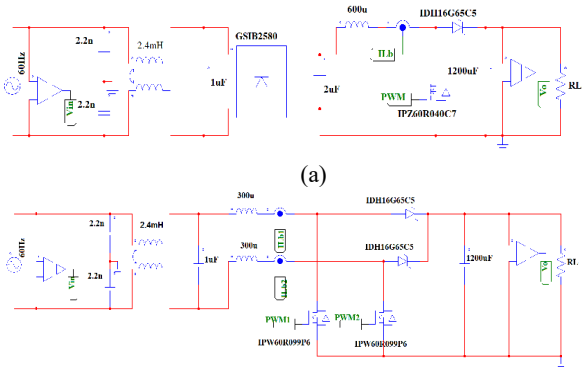
(a) (b)

Fig. 14. Bridgeless PFC current control system performance with IP controller: (a) bode plot; (b) step response

IV. Modeling and Simulation

A. PSIM models for the PFC converters

The simulation models of the designed PFC converters are performed using the PSIM software, and for the simulation results which is closest to the practical reality, no ideal components are used but the converter's components are selected based on commercializing components from the suppliers for both converters as shown in the simulation models in Fig. 15.

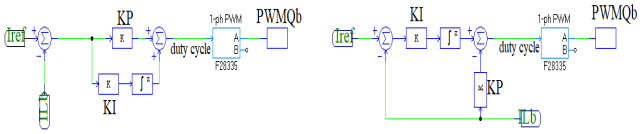


(a)

(b)

Fig. 15. PSIM simulation models for the power circuit of the PFC converters (a) bridge PFC; (b) bridgeless PFC.

A DSP TMS320 F28335 with a DSP speed of 150 MHz and a pulse width modulation (PWM) generator switching frequency of 100 kHz was used to implement the PFC converter's digital control circuit. Because the PI controller is capable of regulating the DC bus voltage to the specified voltage level with good performance, the voltage controller was implemented using the PI in all current loop control scenarios. Figure 16 shows the simulation models of the PI and IP current control loops implemented in PSIM simulation.



(a) (b)

Fig. 16. Implementation of the inner current control circuit in PSIM simulation (a)PI controller; (b)IP controller

B. Simulation results and discussion

With the rating input of 220 Vrms, 60 Hz and full loading condition of 2500 W, and Vo about 400 V, to show the ability of the proposed IP current controller to reduce the ZCD as compared with the conventional PI. The inductor, refence and supply currents as well as the supply voltage are simulated.

With the conventional PI, as shown in Fig. 17, the inductor current was failure to track the reference current at the zero-crossing point, introduce the failure in the input supply current to track the input supply voltage at the zero-crossing point causes ZCD period of about 1.82 ms. On the other hand, Figure 18 shows the inductor current and reference current waveforms of the bridge PFC boost converter with IP controller, demonstrating successful tracking of the inductor current to the reference current as well as the elimination of the ZCD in the input supply current, which decreased from 1.82 to about 0.10 ms.

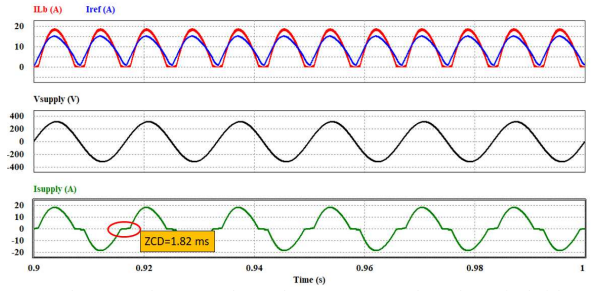


Fig. 17. Inductor, refrence and supply current, supply voltage in bridge PFC with conventional PI

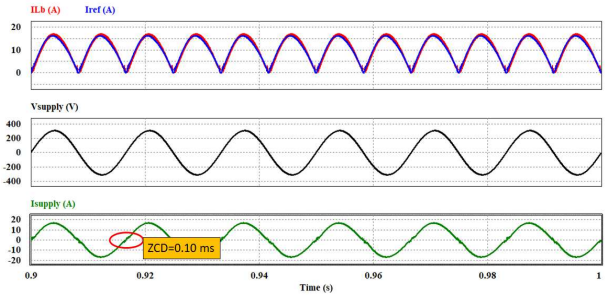


Fig. 18. Inductor, refrence and supply current, supply voltage in bridge PFC with proposed IP

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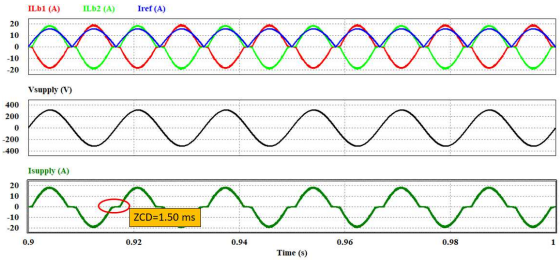

Fig. 19. Inductor, refrence and supply current, supply voltage in bridgeless PFC with conventional PI

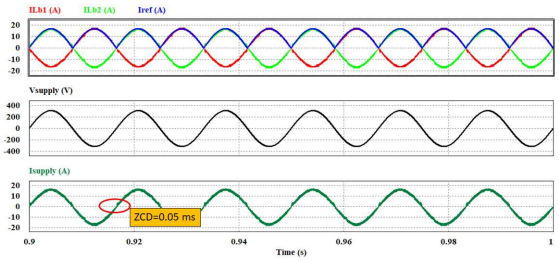

Fig. 20. Inductor, refrence and supply current, supply voltage in bridgeless PFC with proposed IP

Similarly, for the bridgeless PFC converter, the implementation of the IP controller instead of the conventional PI controller in the current control loops reduce the ZCD from 1.50 to 0.05 ms, as demonstrating from the inductor, reference, supply currents and supply voltage shown in Fig. 19 and Fig.20. Figure 21 depicts the THD measurements for the bridge and the bridgeless PFC boost converters with the conventional and the proposed current control techniques and with different loading condition, which shows that the proposed IP controller is sufficient to reduce the THD for both converters to the standard values with different loading conditions. The reducing of the ZCD period with using the proposed IP controller offers bridge and bridgeless PFC converters with lower THD value and hence high-power factor more than 99% and near to unity power factor as depicted in the power factor performance measurements in Fig. 22 for the bridge and the bridgeless PFC boost converters.

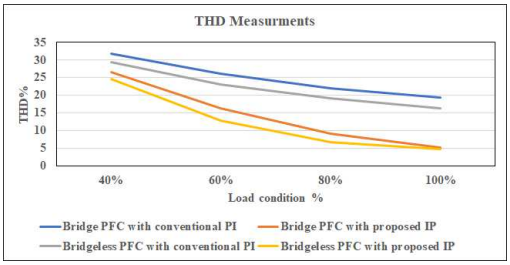

Fig. 21. THD performance comparisons with different controllers

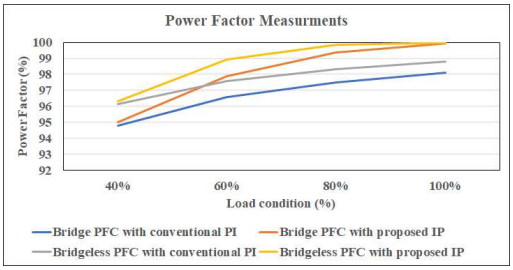

Fig. 22. PF performance comparisons with different controllers

V. Conclusions

In this article, the small-signal models of the bridge and bridgeless PFC boost converters implemented for the telecom power applications are derived. The voltage and current control loops of the bridge and bridgeless PFC converters are optimally constructed utilizing the obtained stability models and appropriate stability criteria. The simulation results of the 2500 W PFC converters show that replacing the conventional PI current controller in the inner current control loops with the proposed IP controller with fast dynamic response improved the performance of the current control loop around the zero-crossing point, reduced the ZCD period, reduced the THD to about 5.11% in the bridge PFC and 4.71% in the bridgeless PFC boost converters, and the input power factor was close to unity in both converters.

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