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Atef K. Allam

Professional Experience	**Assistant Professor** 2005-present: Electrical Eng. Dept., Assiut Univ., Assiut, Egypt. 2010 – present: Computer Engineering Dept., Taibah Univ., Al-Madinah Al-Munawarah, Saudi Arabia. **Postdoctoral Fellow** 2008-present: University of Lyon - Lyon Institute of Nanotechnology (INL) Ecole Centrale de Lyon, France **Research and Teaching Assistant** 2001-2005: Electrical & Computer Eng. Dept., Louisiana State University, Baton Rouge, USA. **Instructor** 2001: Education program in "Egyptian Ministry of Communi-cations & Information Technology (MCIT) ", Egypt. **Teaching Assistant** 1996-2001: Electrical Eng. Dept., Assiut Univ., Assiut, Egypt.
Education	2005: Louisiana State University, Baton Rouge, USA **PhD**, Electrical and Computer Engineering (GPA 4.0/4.0). Major: Computer Engineering, Minor: Computer Science. 2005: Louisiana State University, Baton Rouge, USA **M. Sc**, Electrical and Computer Engineering (GPA 4.0/4.0). 1998: Assiut University, Assiut, Egypt **M. Sc**, Electrical and Computer Engineering. 1994: Assiut University, Assiut, Egypt **B. Sc**, Electrical and Computer Engineering.
Awards	Louisiana State University Graduate Dissertation Fellowship.
Professional Activities	▪ Co-founder of Embedded System Research Lab at Assiut University. ▪ Library for the Optical Network-on-Chip (ONoC ver 2.0) integrated inside the STMicroelectronics simulation environment "OCCS GenKit". ▪ Keynote Speaker: Engineering Between Theory and Practice Conference, "Embedded Systems", Assiut University, Egypt, May 2007. ▪ Passed the "Multi-core Programming for Academia" course from Intel Software College, Dec 2007. ▪ Invited talk, "Optical Network-on-Chip Functional Models and Simulation", Network Architecture Group, STMicroelectronics Co., Catania, Italy, Feb 23, 2009.
Research Interests	▪ Embedded systems Design. ▪ System-Level Design with SystemC and TLM Methodology ▪ Systems-on-Programmable-Chips. ▪ Networks-on-Chip (NoCs). ▪ Microprocessor Interfacing and Microcontroller applications.

Book Chapter	• Atef Allam and Ian O'Connor, "A Protocol Stack Architecture for Optical Network-on-Chip: Organization and Performance Evaluation" Book Chapter in:"Integrated Optical Interconnect Architectures for Embedded Systems", Springer 2013, ISBN: 978-1-4419-6192-1, Ian O'Connor (Editor), Gabriela Nicolescu (Editor).
Recent Publications	• Atef Allam, Ian O'Connor, "A Protocol Stack Architecture for Optical Network-on-Chip", 1st Taibah University International Conference on Computing and Information Technology Al-Madinah Al-Munawarah, Saudi Arabia, 12-14 March 2012.
	• Atef Allam, Ian O'Connor, and Wim Heirman, "Performance Evaluation for Passive-Type Optical Network-on-Chip," IEEE International Symposium on Rapid System Prototyping (RSP). June 8, 2010.
	• Atef Allam, Ian O'Connor, and Alberto Scundurra, Optical Network-on-Chip Reconfigurable Model for Multi-Level Analysis," IEEE International Symposium on Circuits and Systems (ISCAS). 2010.
	• Atef Allam, Ian O'Connor, et al., "Optical NOC Design-Parameters Exploration and Analysis," IEEE International Conference on Electronics, Circuits, and Systems, ICECS. 2009.
	• Atef Allam, J. Ramanujam, G. Baumgartner, and P. Sadayappan, "Memory Minimization for Tensor Contractions using Integer Linear Programming," Proc. Workshop on Performance Optimization for High-Level Languages and Libraries (POHLL-06), held in conjunction with the 20th IEEE International Parallel & Distributed Processing Symposium (IPDPS 2006), Rhodes, Greece, April 2006.
	• Atef Allam and J. Ramanujam, "Simultaneous Peak and Average Power Optimization in Synchronous Sequential Designs Using Retiming and Multiple Supply Voltages," International Conference on IC Design and Technology (ICICDT), Padova, Italy, May 2006.
	• Atef Allam and J. Ramanujam, "Modified Force Directed Scheduling for Peak and Average Power Optimization Using Multiple Supply Voltages," International Conference on IC Design and Technology (ICICDT), Padova, Italy, May 2006.
	• Atef Allam and J. Ramanujam, "Dynamic Memory Usage Optimization using ILP," In Proc. of International Computer Engineering Conference: New Technologies for the Information Society (ICENCO), Cairo, Egypt, Dec 2006.
	• Atef Allam and J. Ramanujam, "ILP and Iterative LP Solutions for Peak and Average Power Optimization in HLS," In Proc. of International Computer Engineering Conference: New Technologies for the Information Society (ICENCO), Cairo, Egypt, Dec 2006.
	• "Optical Network-on-Chip Design Specifications", European FP7 Information and Communication Technologies program, "WADIMOS" project, Lyon Institute of Nanotechnology, France, Jan 21-22, 2009.
Workshops:	• "Performance exploration and scalability analysis", European FP7 Information and Communication Technologies program, "WADIMOS" project, Ghent University, Belgium, Jan 15-16, 2010.

Teaching Experience	**Teaching:**

- Computer Organization
- Computer Architecture
- Modeling and Simulation
- MPSoC Modeling with SystemC (for PhD students)
- Microprocessor Design and Modeling with VHDL
- Computer Networks.
- Operating Systems.
- Object-Oriented Programming (Java and C++)
- Microprocessor Interfacing
- Digital Design
- System Analysis
- Numerical Analysis
- Programmable Logic Controllers

Co-supervised in several senior graduation projects:

- Android Automated Attendance Reporting System using Bluetooth Device Detection, Taibah University, 2013.
- Live Interactive Teaching Environment, Taibah University, 2011.
- PLC : Operating, Programming and Application to Industrial Process, 2000
- Design of Digital and Analog Magnetic Levitation System,1998.

University Services	▪ 2006-2007 Member, Board of Directors, Department of Electrical Engineering, Assiut University. ▪ 2006 Member, Electrical-Engineering Graduate Course Specification Committee (Computer area), Assiut University.
Other Professional Experience	▪ have a direct and strong experience in dealing with many design packages such as Xilinix EDK, Xilinix ISE, MPLAB IDE, MATLAB as well as Object-Oriented programming language. Using VHDL, I have designed, simulated, and implemented a working microprocessor into Xilinx FPGA platform. As such, this has led to strong experience in both hardware and software and their interaction.