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Design and Optimal Control of a Two-Stage Efficient and High PF AC-DC Converter for High-Power Density Industrial Applications

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***Abstract*—power quality is an essential consideration in design of the power supply in high power industrial applications. Thus, this paper covers the design of the different magnetic components, switching element selection considerations, and the voltage current controllers optimal design on the basis of small-signal stability modeling and an adequate stability criterion to enhance the high-power factor (PF), high efficiency and lower current distortions. The proposed converter contains two stages, the power factor correction (PFC) stage and the isolated phase-shift PWM zero-voltage switching (ZVS) DC-DC converter stage. The proposed two-stage converter's total harmonic distortions (THDs), voltage and current ripples, conversion efficiency, and PF performance are investigated using PSIM simulations under various operating conditions. This study designs an industrial 2000 W, 54 V telecom AC-DC supply with a PF of more than 99%, a THD of about 5 %, and conversion efficiency of around 93% at full load.**

Keywords—interleaved PFC, phase shift PWM, ZVS, small-signal modeling, stability criteria, losses distribution.

I. INTRODUCTION

The largest deployment of 5G technology in telecom power applications has led to an increase in the use of universal electronic devices. Due to the fact that this universal electronic equipment often operates on DC power, hence, the rectification process of the AC supply voltage is required. These devices can be powered by conventional AC-DC rectifiers, but their use in high power density applications is constrained by their poor performance characteristics, such as delayed dynamic response to load change, poor regulation, high THD, and low input power factor. Recently, where more efficient power converters are needed, an high efficiency and high PF AC-DC power supply was modified. Recently, it was found that using AC-DC converters with two stages is the best option for preserving high PF and high conversion efficiency [1, 2].

The achieving of high input PF necessitates controlling the supply current's form to follow the supply voltage in order to lower the displacement factor and distortion factor while keeping the PF at high levels [3]. Thus, the PFC converter stage creates the front stage of two-stage AC-DC converters. It can be implemented using a variety of circuit topologies, including the traditional topology for simple construction and control, the interleaved topology for lower ripple current and reduced electromagnetic interface (EMI) level, and the bridgeless PFC topology for the highest efficiency [4, 5].

Most of these PFC topologies use boost converter operation, with voltage and current control loops to regulate the output voltage to the appropriate level and manage the input supply shape. In order to create a converter with good performance, both control loops should be designed optimally. For the purpose of adjusting the DC bus voltage of the PFC converter stage to the appropriate levels (usually 45–63 V DC) for the telecom and communication applications, the second stage of AC–DC converters is implemented and used for such these applications [6].

Depending on the power application, the second stage is implemented as a step-down DC-DC converter stage that can be built as either an isolated converter or a non-isolated topologies. For the reason of the insulation requirements between the load side and the high voltage side of the PFC bus voltage, the isolated converter is more frequently utilized in telecom power applications [7]. Additionally, isolated DC-DC converters based on the phase-shift PWM switching technique have lately risen to the top of the list of techniques due to their capacity to reduce switching losses and offer improved regulation across a wide load range [8, 9].This is certainly relevant when ZVS operation is available for converter switches. The ZVS operation, which has minimal switching losses and low voltage stress, enables also, power conversion with high power density, the design of such these converter topologies must consider the high frequency transformer's design and selection in order to deliver ZVS over a wide load range and reduce switching and conduction losses.

As stated above, a major goal of design an efficient and high PF power supply is to optimize the control loop design in the PFC boost converter circuit. Additionally, the ZVS operation over a wide load range is made possible by the proper design and selection of the power components of the DC-DC converter stage, which lowers the voltage and current stresses, lowers conduction and switching losses, and maintains the efficiency at the highest possible level.

The design procedure of the various power components, and the optimal design of the control circuits of both stages in AC-DC telecom power supply shown in Fig. 1 consisting of the interleaved PFC converter and the isolated phase shift PWM DC-DC converter with ZVS operation are presented in this paper. The proposed power supply's performance is validated using PSIM simulations and compared to previously designed power supplies for the same power applications.

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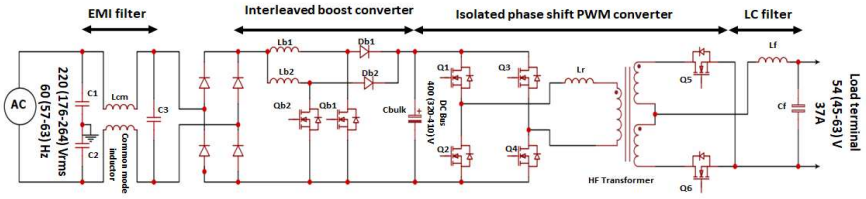


Fig. 1. Overall circuit of the proposed high-power density two-stage telecom AC-DC power supply.

TABLE I. DESIGN SPECIFICATIONS OF THE TARGET CONVERTER

Parameter	Value	Unit
AC supply voltage (V_s)	220 (176-264)	V
AC supply frequency (f)	60 (57–63)	Hz
DC bus voltage (V_{bus})	400 (320–410)	V
Load voltage (V_o)	54(45-63)	V
Rated power (P)	2	kW
Target overall efficiency (η)	>93%	-
Target input PF	>99%	-
Switching frequency (F_{sw})	100	kHz

II. POWER COMPONENTS DESIGN IN BOTH STAGES

Table I shows the design specifications of the employed telecom power supply. The following subsections present the mathematical design of the main power components in both stages.

A. PFC boost Inductors (L_{b1}, L_{b2})

The interleaved boost converter that is employed is made to operate with AC supply voltage with wide range from 176V to about 264V RMS, and the PFC stage power components are designed and selected to works efficiently even at the low voltage level, thus, the operating duty cycle (D_{on}) is computed as follows:

$$D_{on} = \frac{V_{bus} - V_{s\,min} \times \sqrt{2}}{V_{bus}} \tag{1}$$

The value of the boost inductance is determined based on the required circuit ripple current value, which can be estimated as a percentage (about 30%) of the rated current as:

$$\Delta I_{Lb\,rpk} = \frac{P \times \sqrt{2} \times 0.30}{V_{in\,min} \times \eta \times k} \tag{2}$$

For interleaved boost converters, the factor k is presents the normalized converter ripple current factor and can be calculated as follows:

$$k = \sum \begin{matrix} \frac{1-2D_{on}}{1-D_{on}} & for \;\; D_{on} \le 0.5 \\ \frac{2D_{on}-1}{D_{on}} & for \;\; D_{on} \ge 0.5 \end{matrix} \tag{3}$$

Hence, in interleaved boost converters, the boost inductors value can calculate as:

$$L_{b1} = L_{b2} = \frac{V_{in\,min} \times \sqrt{2} \times D_{on}}{\Delta I_{Lb\,rpk} \times F_{sw}} \tag{4}$$

B. DC bus capacitor

The DC bus capacitor or the bulk capacitance value (C_{bulk}) is calculated based on the basis of the specified DC bus ripple voltage ΔV_{rpp} which usually not more than 20V for the telecom power applications as expressed:

$$C_{bulk} \ge \frac{P_o}{2 \times \pi \times f_{min} \times \Delta V_{rpp} \times V_{bus}} \tag{5}$$

C. High frequency (HF) transformer

According to the DC-DC converter maximum operating duty cycle (d_{max}) at the minimum DC bus voltage rating, the transformer turns ratio (a) is determined as follows:

$$a = \frac{N_P}{N_S} = \frac{V_P}{V_S} \tag{6}$$

Let d_{max} be about 70% and minimum DC bus voltage is 320V. the ratio a is determined as:

$$a = \frac{V_P}{V_S} = \frac{(V_{bus\,min} - 2V_f) d_{max}}{V_o + V_f} = 4.1 \tag{7}$$

where V_f is the primary switch forward voltage drop, which in calculations is set to be 0.5V. For HF transformer with turns ratio of 5, the formula for calculating the DC-DC converter stage's effective operating duty cycle (d_{eff}) is:

$$d_{eff} = \frac{(V_o + V_f) a}{(V_{bus} - 2V_f)} = 0.675 \tag{8}$$

The maximum magnetizing inductance to realize ZVS is used to design the transformer magnetizing inductance (L_m) [6, 10].

$$L_m = \frac{T_{dead}\, a\, V_{o\,min}}{C_{HB}\, V_{bus\,min}} * \left(\frac{T_{s\,min}}{4} - \frac{T_{dead}}{2} \right) \tag{9}$$

where C_{HB} is the primary switch's equivalent capacitance, which can be found on its datasheet. The $T_{s\,min}$ and T_{dead} are the minimum switching and the PWM dead times respectively, which may be estimated based on the determined effective duty ratio value.

Efficiency, thermal expansion, frequency, eddy currents, and core losses are the primary factors to consider when selecting the HF transformer core material and dimensions. Iron powder cores, ferrite cores, and the amorphous steel cores can all be used in high-frequency applications (10kHz-3MHz). Ferrite cores are effective insulators that reduced the losses and eliminate the eddy currents and reduced core loss. The HF transformer core selection technique can start with a core weight, effective volume, or effective area according to the designed power rating and the operating switching frequency, and then choose the core that best fits these parameters.

In this study, the ferrite core provided by the TDK Company is deemed to be excellent for the HF DC-DC converters in high power applications. It has a PQ form and an effective area (A_e) of roughly 200mm^2. Typically, the magnetic flux of the designed HF transformer should be kept at a low level to achieve acceptable core losses (0.1-0.4Tesla). Since we set a 0.35Tesla upper limit on the highest magnetic flux (B_{max}), the primary turns (N_p) is calculated as follows:

$$N_P = \frac{V_{bus} \times d_{eff}}{2 \times B_{max} \times A_e \times f_{SW}} = 19.10\; Turns \tag{10}$$

The operating maximum magnetic flux of the designed HF transformer with N_p=20 turns is calculated to be around 0.336Tesla.

D. Output filter inductor

The specified filter ripple current I_{Lf}, calculated as a percentage (about 15%) of the rated load current, and forms the basis for the filter inductance value L_f calculation. the L_f value can be determined by applying KVL to the synchronous rectification circuit as given in the following formula:

$$L_f = \frac{V_{load}(1-d_{eff})}{\Delta I_{Lf} * f_{SW}} \quad (11)$$

E. Output filter capacitor

The filter capacitance value C_f is calculated using the specified load ripple voltage ΔV_{Ripple} which usually not more than 200 mV for the telecom power applications, as well as the needed hold-up time ($t_{hold-up}$), which is defined as the time it takes the load filter current to reach 90% of the rated load current.

$$C_f = \frac{0.9 I_{load} * t_{hold-up}}{\Delta V_{Ripple}} \quad (12)$$

F. Resonant inductor

The size of the resonant inductance (L_r)value is determined based on the required amount of energy necessary to achieve the ZVS state. Therefore, the energy provided by the parasitic capacitance of the primary switches (C_{oss}) as well as the energy from the transformer winding capacitance (C_w) must be able to be exhausted by L_r and transformer leakage inductance (L_{lk}).

$$\frac{1}{2} I_{P\,rms}^2 (L_r + L_{lk}) \geq \frac{4}{3} C_{oss} V_{bus}^2 + \frac{1}{2} C_w V_{bus}^2 \quad (13)$$

G. Switching elements selection

There are several crucial selection considerations, which may be summarized as given in Table II , that must be taken into account in order to select an ideal switching component for both stages in the proposed two stage power supply to reduce the conduction and switching losses, and also to offers the ZVS operation of the converter switching elements.

The design results as well as the selected switching elements for both stages in the designed power supply introduced in this work are given in Table III.

III. CONTROL CIRCUITS DESIGN AND IMPLEMANTATION IN BOTH STAGES

A. Interleaved PFC control loops design

Figures 2 and 3 shows the interleaved PFC equivalent circuit and the proposed control loops respectively.

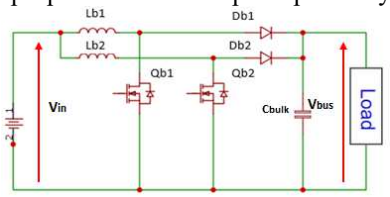


Fig. 2. Equivalent circuit of the interleaved boost converter unit.

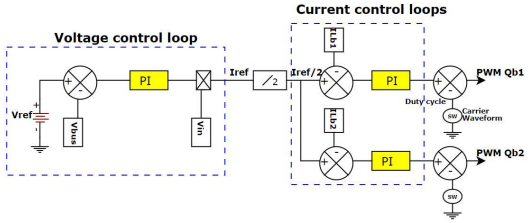


Fig. 3. Implemantation of the PFC stage control circuit.

TABLE II. DESIGN CONSIDERATIONS OF THE POWER SUPPLY SWITCHING ELEMENTS

Stage	Switching Element	Design considerations
Interleaved PFC converter stage	Mosfets Q_{b1}, Q_{b2}	• Low output capacitance and small $Rds_{on\ to}$ reduce conduction losses. • Fast turn-on/off switching to reduce device switching losses. • High dV_{dS}/dt and high dI_F/dt to withstand transit and overshoots. • Small thermal resistance to reduce thermal losses.
	Diodes D_{b1}, D_{b2}	• low reverse recovery time (t_{rr}), and low reverse recovery charge (Q_{rr}) to reduce reverse recovery losses.
Phase shift PWM DC-DC converter stage	Primary Mosfets Q_1-Q_4	• Low output capacitance and small $Rds_{on\ to}$ reduce conduction losses. • Fast turn-off switching and higher gate plateau voltage to reduce switching losses. • Low capacitance at the output (C_{oss}) to support a wider ZVS range and less deadtime. • High dV_{dS}/dt and high dI_F/dt to withstand spikes and overshoots. • Low thermal resistance to reduce thermal losses. • Low reverse recovery charge.
	Secondary Mosfets Q_5, Q_6	• Very small R_{dson} as possible to reduce switching and conduction losses (due to high current stress in secondary side).

TABLE III. POWER COMPONENTS DESIGN RESULTS

Component	Value/Description
PFC boost Inductors	300uH
DC bus capacitor	1200uF
HF transformer	PQ 40/40 core, a=20:4:4 L_m=2.8mH
Output filter inductor	30uH
Output filter capacitor	3300uF
Resonant inductor	31uH
Mosfets Q_{b1}, Q_{b2}	IPZ60R040C7
Diodes D_{b1}, D_{b2}	IDH16G65C5
Primary Mosfets (Q_1-Q_4)	IPW60R070CFD7
Secondary Mosfets (Q_5, Q_6)	IPP110N20N3

The circuit operation principle can be presented using the small signal model in the state space matrix form as given.

$$\begin{bmatrix} i_{Lb1} \\ i_{Lb2} \\ v_{bus} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{(1-d)}{L_{b1}} \\ 0 & 0 & -\frac{(1-d)}{L_{b2}} \\ \frac{(1-d)}{C_{bulk}} & \frac{(1-d)}{C_{bulk}} & -\frac{1}{R\,C_{bulk}} \end{bmatrix} \begin{bmatrix} i^*_{Lb2} \\ i^*_{Lb1} \\ v^*_{bus} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{b1}} & \frac{v_{bus}}{L_{b1}} \\ \frac{1}{L_{b2}} & \frac{v_{bus}}{L_{b2}} \\ 0 & \frac{i_{L1}+i_{L2}}{C_{bulk}} \end{bmatrix} \begin{bmatrix} v^*_{in} \\ d^* \end{bmatrix} \quad (14)$$

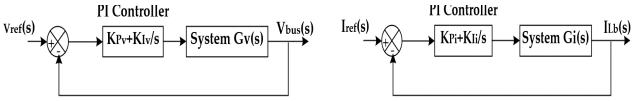
To derive the DC bus voltage and inductor current's open loop TFs, the Laplace transform is applied to (14) as follows:

$$G_v(s) = \frac{v^*_{bus}(s)}{i^*_{Lb1,2}(s)} = \frac{|v_{in}|}{2V_o\ Cbulk\ s} \quad (15)$$

$$G_i(s) = \frac{i^*_{Lb1,2}(s)}{d^*(s)} = \frac{\left(\frac{V_o}{Lb_{1,2}C_{bulk}R}\right).(sRC_{bulk}+2)}{s^2+\frac{1}{C_{bulk}R}s+\frac{2}{Lb_{1,2}C_{bulk}}(1-d)^2} \quad (16)$$

At HF switching case, the C_{bulk} can be shorted in which the TF in (16) can be simplified as:

$$G_i(s) \cong \frac{2\,V_{bus}}{sL_{b1,2}} \quad (17)$$



(a) (b)

Fig. 4. Closed loops PFC controllers. (a) voltage control loop; (b) current control loop.

Figure 4 depicts a block diagram of the voltage current closed loops of the PFC stage. The closed loops TFs $GCL_v(s)$ and $GCL_i(s)$ can be expressed as:

$$G_{CLv}(s) = \frac{V_{bus}(s)}{V_{ref}(s)} = \frac{\frac{V_{in}}{2\,V_{bus}\,C_b}\cdot(K_{Pv}\,s+K_{Iv})}{s^2+\frac{V_{in}\,K_{Pv}}{2\,V_{bus}\,C_{bulk}}s+\frac{V_{in}\,K_{Iv}}{2\,V_{bus}\,C_{bulk}}} \quad (18)$$

$$G_{CLib1}(s) = \frac{I_{Lb1}(s)}{I_{ref}(s)} = \frac{\frac{2V_{bus}}{L_{b1}}\cdot(K_{Pi}\,s+K_{Ii})}{s^2+\frac{2V_{bus}\,K_{Pi}}{L_{b1}}s+\frac{2V_{bus}\,K_{Ii}}{L_{b1}}} \quad (19)$$

After determining the closed loops TFs, the gains of the PI controllers can be estimated using the general form of the 2nd order system TF and bode plots by choosing the appropriate designed control loop bandwidth and the undamped natural frequency that augmented the optimal stability criteria for the voltage and current control systems' closed loops. To reduce the distortions of the output DC voltage reflected by the AC input voltage at 60Hz, the bandwidth of this control loop must set to be small value. Also, to allow inductors currents to follow the reference current, the bandwidth of the inner current control loop must be significantly higher than that of the voltage control loop. Furthermore, to reject the inductor current distortions at the switching frequency, the current control loop bandwidth must be less than the switching frequency (f_{sw}). According to these design considerations, the undamped natural frequency was assumed to be approximately 0.707 in this work, and the closed loop bandwidths of Wn were assumed to be approximately 100rad/s and 15krad/s for the outer voltage and inner current loops, respectively.

Figure 9 shows a bode plots of the designed control systems, demonstrating that the voltage controller provides unity gain for frequencies less than 32Hz. acting as a low-pass filter to remove the voltage ripple at 60Hz. In addition, for frequencies less than 4900Hz, the current control loops provide unity gains. To remove switching frequency current ripples, this current control loop also acts as a low pass filter.

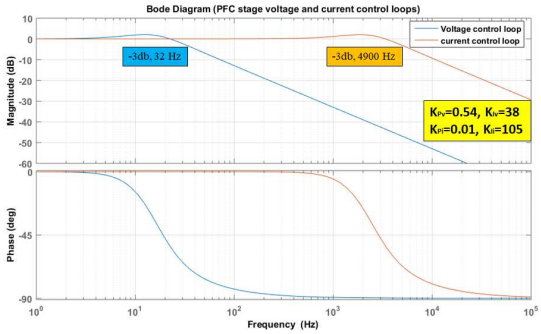


Fig. 5. Bode plots of the closed loops TF of the PFC stage control loops.

Furthermore, the root locus plots for both loops were determined, as shown in Fig. 6, demonstrating that the designed controllers are inherently stable.

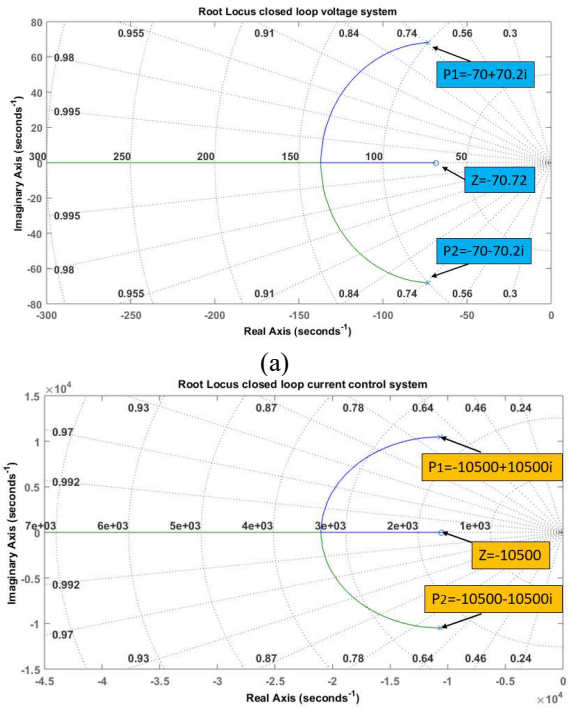


Fig. 6. Eigenvalues location of the closed loops TF of the PFC stage. (a) voltage control loop; (b) current control loop.

B. DC-DC converter control circuit implemantation

Figure 7 depicts the strategy of the control circuit implemented in PSIM software for controlling the Mosfet switches in this converter stage.

The phase-shift PWM approach is used to control the full bridge on the primary side by phase shifting the switching pulses of one half-bridge with respect to the other. In this part, the high power conversion is provided with using the ZVS technique. Both voltage-mode and current-mode control strategies are available for use in this area of the control system. Current-mode-control is common because it is more effective than voltage mode control. However, the current-mode architecture may become unstable when the PWM duty cycle approaches 50%. To eliminate this instability and restore stability across a wide range of the converter operating duty cycles, the converter primary current slope compensation technique is applied with using the ramp signal with 200kHz frequency as shown in the block diagram in Fig. 7 [6, 11].

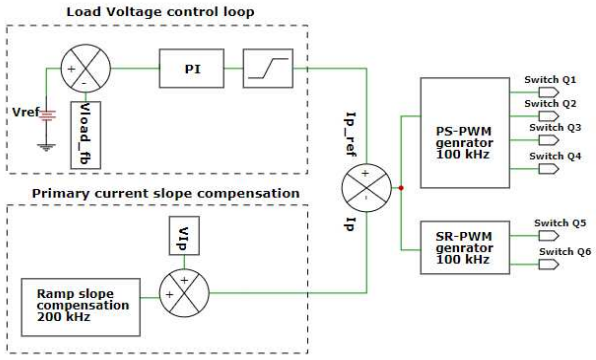


Fig. 7. Implemantation of the DC-DC converter control circuit.

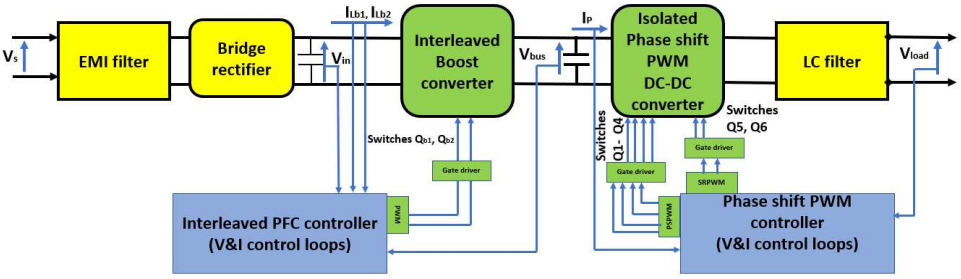


Fig. 8. Overall control strategy of the proposed high-power density two-stage telecom AC-DC converter.

IV. PSIM SIMULATION RESULTS AND DISCUSSIONS

The overall control strategy of the proposed high-power density two-stage telecom AC-DC converter is shown in Fig. 8. The PSIM software is used to assess its performance using the optimal voltage current control loop and both stages' power components listed in Table III. To evaluate the effectiveness of the PFC stage current control loop that was best developed, using a 2kW full load and a rated supply voltage of 220V RMS, 60Hz. The simulation waveforms of the voltages currents and supply PF are displayed in Fig. 9. It is noticed that the inductors' currents are successfully made to follow the reference current by the specified control loops, resulting in a less than supply voltage current 5-degree phase difference and a minimum PF of about 99.75%.

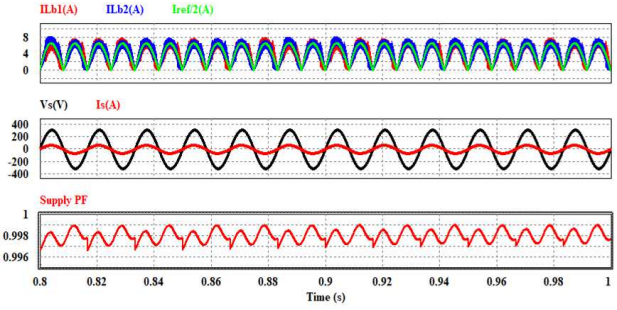


Fig. 9. Voltages-currents and input PF waveforms at full load.

As shown in Fig. 10, the DC bus and AC supply voltages are simulated to investigate the designed voltage controller's dynamic response and reliability to regulate the voltage to the specified value (400V) with the specified ripple contents ($15V_{rpp}$) over a wide range of an operating AC supply voltages from 176V to 264V RMS and at full load condition.

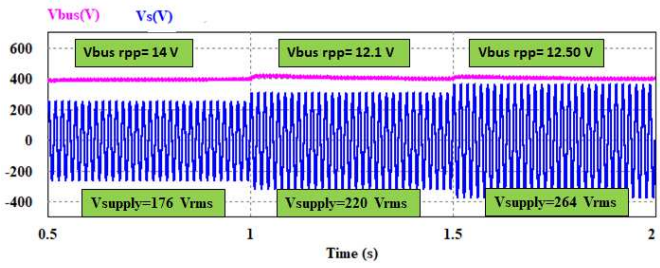


Fig. 10. DC bus voltage with different AC voltage and ripple measurement.

Figure 11 illustrates the voltage current operating waveforms of Mosfets Q_1 and Q_3 on the primary side of the converter. This shows that the designed converter control loops and the used resonant inductance value are sufficient to enable ZVS operation for the DC-DC converter switches, which reduced the switching losses and increase the stage efficiency.

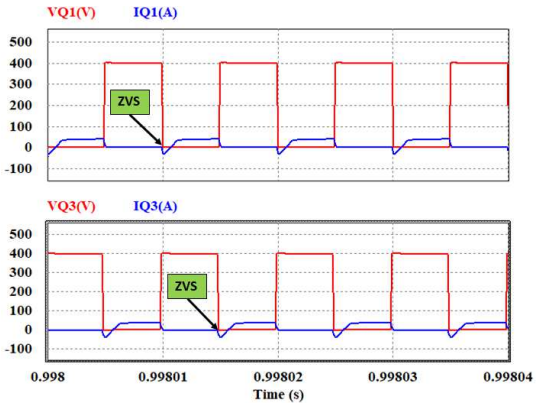


Fig. 11. Waveforms of the voltage and current of the primary switches.

Figure 12 depicts the load voltage and current waveforms, as well as measurements of the ripple content. The designed LC filter on the phase-shift PWM converter's output load side keeps the load voltage and current ripple to about 13.5mV and 20mA respectively. Also, DC bus voltage is regulated to 400V with a ripple of 12.1V at 220V.

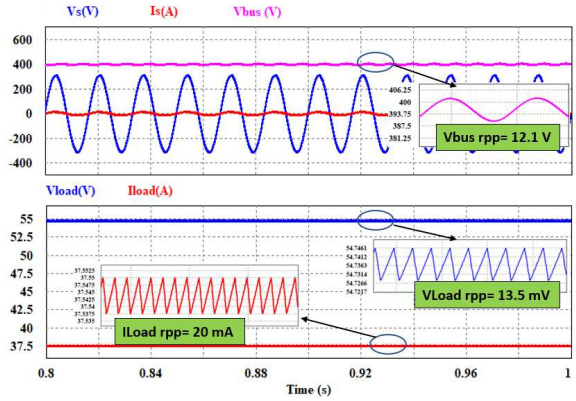


Fig. 12. Supply, DC bus and load voltage current waveforms at full load.

FFT analysis is performed to the supply current waveform at full load condition with fundamental frequency of 60Hz as given in Fig. 13 to reveal the THD in the supply input current under rated input voltage and rated output power. The results as shown in Fig. 13 reveals that the fundamental current, which is approximately 13.08A measured at 60Hz, and the third harmonic current, which is approximately 0.262A measured at 180Hz. The THD, as measured, is approximately 2.65% which is less than the standard limits for the telecom power supplies.

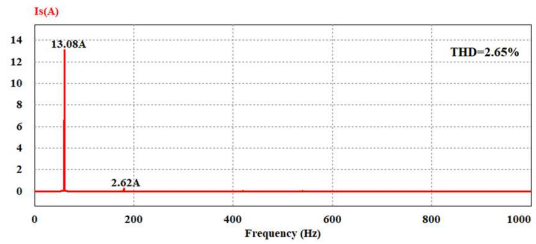


Fig. 13. Supply current FFT analysis at full load.

As depicted in Fig. 14, the distribution of power losses across the various power components is estimated using the PSIM simulation at full loading condition. With a budget of around 18%, the secondary Mosfets contributed the most to the power supply's losses. The filter inductor and bridge rectifier came in next with a budget of about 16% each, and the primary Mosfets came in at about 12%. The efficiency of the proposed power supply at full load is about 94.50%.

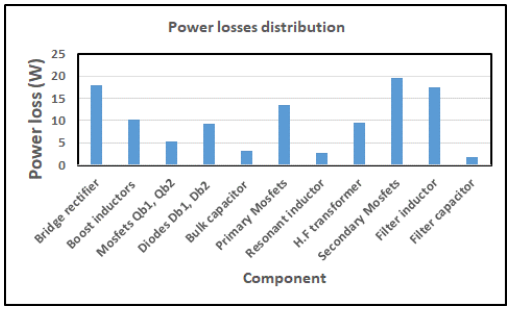


Fig. 14. Power losses distribution in the designed power supply.

Table IV compares the performance of the designed power supply with commercialized two-stage power supplies for telecom server power applications. The performance of all power supplies introduced in the table is determined at full load, and rated input voltage condition. It can be observed that the designed power supply offers high power density power conversion with PF near unity, high conversion efficiency, and extremely low THD value as compared with the previously designed power supplies with different design topologies.

TABLE IV. PERFORMANCE COMPARISION OF PROPOSED POWER SUPPLY WITH PREVIOUS WORK.

Design	Topology	P (W)	η (%)	PF (%)	THD (%)
Proposed	Interleaved PFC PS-ZVS converter	2000	94.50	99.75	2.65
[11]	Traditional PFC PS-ZVS converter	2000	93.15	99.35	5.50
[12]	Traditional PFC LLC converter	800	94.47	99.50	2.00
[13]	Bridgeless PFC LLC converter	1000	96.99	96.20	8.96
[14]	Interleaved PFC LLC converter	500	94.55	99.00	8.00
[15]	bridgeless PFC LLC converter	1600	94.20	98.90	4.00

V. CONCLUSIONS

A two-stage AC-DC power supply that is suitable for supplying high power to 5G telecom power applications is proposed in this paper. The mathematical design, optimal selection of the power components, and the optimal control technique of the voltage current control loops of the proposed power supply are described. The interleaved PFC control loops are optimally designed AC according to a suitable stability criterion, resulting in an input supply with a PF of more than 99.75% and a THD of approximately 2.65% at full loading. Furthermore, the converter's power switches and magnetic power components are designed to offer the switching operation with ZVS, which reduces switching losses and provides high conversion efficiency.

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