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Design of Wide Input Voltage Range and High PF Two-Stage AC-AC Converter Suitable for Inductive Loads

유도 부하에 적합한 넓은 입력 전압 범위와 높은 역률의 2단 AC–AC 컨버터 설계

Ahmed H. Okilly · Jeihoon Baek

아메드하싼오킬리[*] · 백제훈[†]

Abstract

In this paper, a two-stage AC-AC power supply is designed to specifically handle the operation and performance improvements of the power system with highly inductive loads. The proposed power supply scheme includes an input interleaved power factor correction (PFC) stage to improve the input power factor (PF) and regulate the DC bus voltage required for the second stage, which is a voltage source inverter (VSI) with an output low pass filter to adjust the load harmonics contents and regulate the load voltage and frequency to the specified AC load values. The small-signal models of the PFC and VSI stages are obtained, and optimal voltage and current control loops for both stages are designed based on the obtained models to improve the required system power performance and stability. PSIM simulation is used to examine the performance of the proposed power supply under various input-output operation conditions. This work achieves a 500VA, (180-260)V RMS Power supply with an input PF of 99%, better output voltage regulation, and a lower THD value for the purpose of supplying industrial inductive loads.

Key Words

AC power supply, Inductive load, Small signal models, PFC, VSI with LC filter, Power factor, THD

1. Introduction

The reactive power required for magnetization increases the amounts of required supply apparent power to the distribution system in industrial inductive loads such as electric motors, inductors, transformers, and contactor coils. The input PF will be reduced as the supply reactive and apparent power are increased. Reduced PF causes larger conductors, large copper losses, poor voltage regulation, and a reduction in system power and current capacity [1].

Many techniques have recently been used to improve system power performance and stability with these loads, such as reactive power compensation techniques using flexible AC transmission systems (FACTS) devices such as static var compensator (SVC), static synchronous series compensator (SSSC), and static synchronous compensator (STATCOM), which are used to improve system operation and stability by controlling the active-reactive power flow on the power grid with such these loads. Active power filters also widely used current injection and reactive power compensation to aid in harmonic current compensation [6], [7].

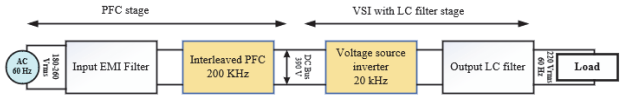

Fig. 1 Structure of the proposed two-stage AC-AC converter

As shown in Fig. 1, a two-stage AC-AC power supply based on rectifying AC power into DC and then DC into AC with an inverter circuit can be used to control the input PF, reduce THD values at the supply and load sides, and regulate the voltage and frequency to distribution levels which capable of handling the operation of the power system with such loads.

The power factor correction stage (PFC) is the first stage of the power supply and usually implements two control loops,

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one for the current to keep the phase shift between the supply voltage and current waveforms at the lowest value and thus keep the input power factor at the highest value, and another for the voltage to keep the output voltage at the required DC bus voltage. Many PFC converter circuit typologies are presented in [8], [9].

Most of these typologies are based on the boost converter operation principle, such as conventional boost PFC, interleaved boost PFC, and bridgeless boost PFC converters. When compared to conventional and bridgeless PFC boost converters, the interleaved PFC boost converter provides conversion with input ripple current cancellation, which reduces current THD, current stress in the converter components, power losses, and increases conversion efficiency. Furthermore, interleaving the input current into two channels and collecting it again on the output side reduces thermal stress in the converter components, improving thermal performance and increasing conversion capacity [9]-[12].

The proposed power supply's second stage is implemented as a voltage source inverter (VSI), which has recently been used to improve power quality in many industrial applications [13]-[15]. A VSI with optimally designed two control loops and an LC filter can be used to convert the front stage's DC bus voltage to the required AC distribution level on the load side, as well as to maintain harmonics contents and ripple current values at the specified levels.

The rest of this paper is organized as follows: Section 2 describes the design of the power components used to derive the small-signal model based on the averaging small signal stability technique, as well as the voltage and current control loops of the interleaved PFC stage. Section 3 presents the small-signal model of the VSI stage, control loops designed using the Ziegler Nichols closed-loop tuning technique, and the optimal design of the LC filter components. Section 4 displays the modeling and simulation results for the proposed two-stage power supply. Section 5 is the conclusion of the paper.

2. Interleaved PFC Stage

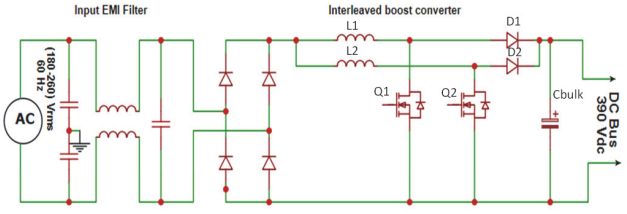


Fig. 2 Schematic circuit of the interleaved PFC stage

Figure 2 depicts the schematic circuit of the employed power supply's front stage, which is a 2-channel interleaved PFC boost converter stage comprised of an EMI filter, a bridge rectifier, and a symmetric 2-unit of a single-phase boost converter operating with a 180-degree phase shift.

The interleaved PFC boost converter's operation principle is based on the operation of the 2-channel interleaved boost converter shown in Fig. 3. The interleaved boost converters, inductors, and bulk capacitor must be optimally designed in order to keep the voltage and current ripples within the limits specified in the following subsections.

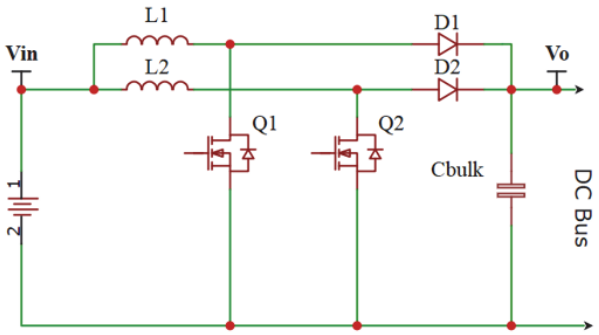


Fig. 3 Schematic circuit of the interleaved boost converter

2.1 Interleaved Boost inductors and bulk capacitor design

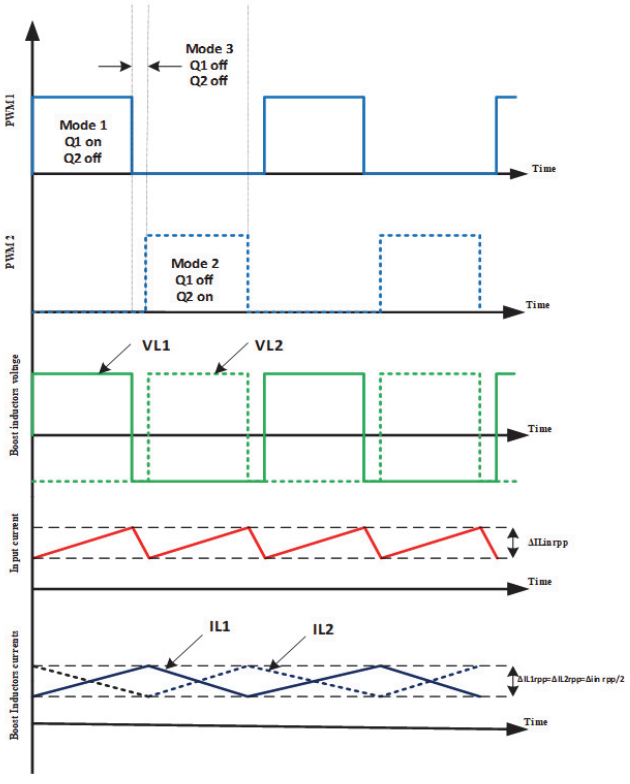


Fig. 4 Voltage and currents wave forms of the PFC stage

Given that the 2-unit is symmetric and that the PWM of each unit has a 180-degree phase shift. The circuit operation of the designed interleaved boost converter working in continuous current conduction mode (CCM) can represent four operating modes, and if the average duty cycle is less than 0.5, both switches will not be turned on at the same time, resulting in three operating modes that describe the on-off states of the 2-channel switches as depicted in the converter waveforms in Fig. 4, where V_{L1}, V_{L2} represent inductors voltages and I_{L1}, I_{L2} represent the inductors currents.

The employed interleaved boost converter is designed to work with a wide range of input AC supply voltages ranging from 180V to approximately 260V rms, and the power components of the boost converter unit are designed to offer good performance with the lowest input voltage level where the operating duty cycle can be calculated as:

$$D_{on} = \frac{V_o - Vin\min \times \sqrt{2}}{V_o} \tag{1}$$

The boost inductor ripple current peak to peak value can be calculated as the percentage (% Ripple) of the converter total input current.

$$\triangle I_{L\ rpk} = \frac{P_{out} \times \sqrt{2} \times \%Ripple}{Vin\min \times \eta \times K} \tag{2}$$

The variable K is defined as the normalized input ripple current factor for interleaved boost converters and can be calculated as follow:

$$K = \sum \begin{matrix} \frac{1-2D}{1-D} & \text{if } D \le 0.5 \\ \frac{2D-1}{D} & \text{if } D \ge 0.5 \end{matrix} \tag{3}$$

For the interleaved boost the boost inductor at each channel can calculated as:

$$L_1 = L_2 = \frac{Vin\min \times \sqrt{2} \times D_{on}}{\triangle I_{L\ rpk} \times F_{sw}} \tag{4}$$

The output capacitor value usually calculated to meet the specified output voltage ripple using (5), also, this value should be enough to deliver the output minimum voltage hold up with the specific time (t_{hold}), as given in (6) where V_{rpp} is the peak to peak output voltage ripple. The larger value among the two equations was selected to design the output capacitor.

$$C_{bulk} \ge \frac{P_o}{2 \times \pi \times F \times V_{rpp} \times V_o} \tag{5}$$

$$C_{bulk} \ge \frac{2 \times P_o \times t_{hold}}{V_o^2 - V_{o\min}^2} \tag{6}$$

Using the converter parameters given in Table 1, the required boost inductors, and bulk capacitance for the interleaved boost converter can be obtained.

Table 1 Design specifications of the PFC stage

Design Specifications		
Parameter	Value	Unit
Supply voltage (Vin)	220 (180-260)	V
Supply Frequency (F)	60	Hz
Output Voltage (Vo)	390 (320-410)	V
Rated Power (Po)	300	W
Desired Efficiency (η)	95%	-
Switching Frequency (Fsw)	200	kHz
Hold Up Time (thold)	10	ms
Inductor ripple (% Ripple)	30%	
voltage ripple (Vrpp)	16	Vpp

2.2 Interleaved boost converter small signal modeling

Assume the interleaved boost converter used in this work is in continuous current conduction (CCM) mode. The mathematical equations that describe the change in inductors currents (I_{L1}, I_{L2}) and output voltage (V_o) in the converter depicted in Fig. 3 are as follow:

$$\frac{dI_{L1}(t)}{dt} = \frac{Vin}{L_1} - \frac{V_o(1-D)}{L_1} \tag{7}$$

$$\frac{dI_{L2}(t)}{dt} = \frac{Vin}{L_2} - \frac{V_o(1-D)}{L_2} \tag{8}$$

$$\frac{dV_o(t)}{dt} = \frac{I_{L1}(1-D)}{C_{bulk}} + \frac{I_{L2}(1-D)}{C_{bulk}} - \frac{V_o}{R\ C_{bulk}} \tag{9}$$

Assume all variables (I_{L1}, I_{L2}, Vin, V_o, and D) are at the steady state at the selected operational point and the small-signal AC variation ($i_{L1}^*, i_{L2}^*, v_{in}^*, v_o^*$, and d^*), where

$$\begin{aligned} &I_{L1} = i_{L1} + i_{L1}^* \ ; I_{L2} = i_{L2} + i_{L2}^*; \\ &Vin = vin + vin^*; V_o = v_o + v_o^* \ ; D = d + d^* \end{aligned} \tag{10}$$

Substituting from (10) in (7)-(9), and with using the averaging small signal technique [9], which assume that over the switching period, the change in the inductor current and the change in

capacitor voltage is equal to zero we obtain

$$\frac{d(i_{L1}^*)}{dt}=\frac{1}{L_1}(vin^*)+\frac{v_o}{L_1}(d^*)-\frac{(1-d)}{L_1}(v_o^*) \tag{11}$$

$$\frac{d(i_{L2}^*)}{dt}=\frac{1}{L_2}(vin^*)+\frac{v_o}{L_2}(d^*)-\frac{(1-d)}{L_2}(v_o^*) \tag{12}$$

$$\frac{d(v_o^*)}{dt}=\frac{(1-d)}{C_{bulk}}(i_{L1}^*)+\frac{(1-d)}{C_{bulk}}(i_{L2}^*) + \frac{i_{L1}+i_{L1}}{C_{bulk}}(d^*)-\frac{1}{R\ C_{bulk}}(v_o^*) \tag{13}$$

Arrange state Equations (11)~(13) in state space matrix form to obtain the state space representation of the interleaved CCM PFC converter's small signal stability model as (14).

$$\begin{bmatrix} i_{L1}^* \\ i_{L2}^* \\ v_o^* \end{bmatrix}=\begin{bmatrix} 0 & 0 & -\frac{(1-d)}{L_1} \\ 0 & 0 & -\frac{(1-d)}{L_2} \\ \frac{(1-d)}{C_{bulk}} & \frac{(1-d)}{C_{bulk}} & -\frac{1}{R\ C_{bulk}} \end{bmatrix}\begin{bmatrix} i_{L1}^* \\ i_{L2}^* \\ v_o^* \end{bmatrix} + \begin{bmatrix} \frac{1}{L_1} & \frac{v_o}{L_1} \\ \frac{1}{L_2} & \frac{v_o}{L_2} \\ 0 & \frac{i_{L1}+i_{L2}}{C_b} \end{bmatrix}\begin{bmatrix} vin^* \\ d^* \end{bmatrix} \tag{14}$$

2.3 Control Circuits Design of the PFC Stage

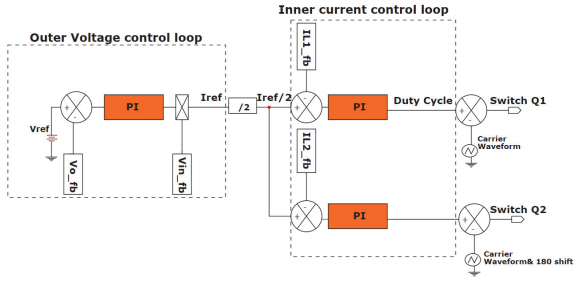


Fig. 5 The structure of the control system of the PFC stage

Using the Laplace transform of the small signal model obtained in (14), the transfer functions (TF) of the output voltage and inner current control systems for the interleaved CCM PFC converter can be obtained as (15), (16). The TF of the PI controllers for the voltage and current control loops can also be expressed as (17). (18).

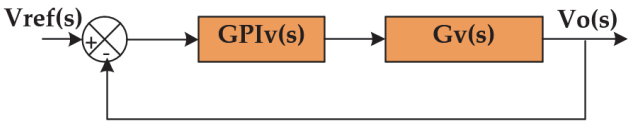
$$G_v(s)=\frac{v_o^*(s)}{i_{L1,2}^*(s)}=\frac{vin}{2\,V_o\ C_{bulk}\ s} \tag{15}$$

$$G_i(s)=\frac{i_{L1,2}^*(s)}{d^*(s)}=\frac{\left(\frac{V_o}{L_{1,2}C_{bulk}R}\right)\cdot(sRC_{bulk}+2)}{s^2+\frac{1}{C_{bulk}R}s+\frac{2}{L_{1,2}C_{bulk}}(1-d)^2} \tag{16}$$

$$G_{PIv}(s)=K_{Pv}+\frac{K_{Iv}}{s} \tag{17}$$

$$G_{PIi}(s)=Kpi+\frac{K_{Ii}}{s} \tag{18}$$

Because the converter switching frequency (Fsw) in this work was chosen to be around 200kHz for the inner current control loops, the capacitor (Cbulk) can be shorted for high frequency analysis, and the open-loop TF of the inductor current system in (19) can be simplified as follows (19).



$$G_{i1}(s)=G_{i2}(s)=\frac{2V_o}{s\ L_{1,2}} \tag{19}$$

Fig. 6 Closed loop voltage control system of the PFC stage

Figure 6 depicts the control blocks of the interleaved PFC stage's closed loop voltage control system. Where the voltage closed loop's TF can be expressed as:

$$G_{clv}=\frac{\frac{v_{in}\ K_{Pv}}{2\,V_o\ C_{bulk}\ s}\ s+\frac{v_{in}\ K_{Iv}}{2\,V_o\ C_{bulk}\ s}}{s^2+\frac{v_{in}\ K_{Pv}}{2\,V_o\ C_{bulk}\ s}+\frac{vin\ K_{Iv}}{2\,V_o\ C_{bulk}\ s}} \tag{20}$$

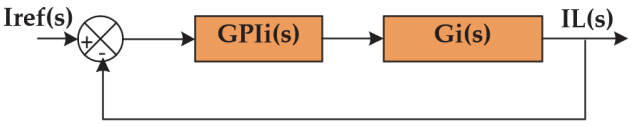


Fig. 7 Closed loop current control system of the PFC stage

Figure 7 depicts the control blocks of the interleaved PFC stage's closed loop current control system. Where the current closed loop's TF can be expressed as:

$$G_{cli}(s)=\frac{\frac{2V_oK_{Pi}}{L_{1,2}}\ s+\frac{2V_oK_{Ii}}{L_{1,2}}}{s^2+\frac{2V_oK_{Pi}}{L_{1,2}}\ s+\frac{2V_oK_{Ii}}{L_{1,2}}} \tag{21}$$

Once the transfer functions of the control loops have been determined, the gains of the PI controller can be obtained using the standard form of the second-order system TF by selecting the appropriate control system bandwidth and undamped natural frequency, which improved the optimal stability criterion. To avoid harmonics of the output DC voltage reflected by the AC

input voltage at 60Hz, the outer voltage loop's bandwidth must typically be very small [9]. Also, the bandwidth of the inner current loop must be greater than that of the outer voltage control loop in order for the inductor current to follow the reference current. In this study, the undamped natural frequency (ξ) was assumed to be around 0.707, and the closed-loop bandwidth values for the interleaved PFC converter's outer voltage and inner current loops were assumed to be around 100rad/s and 50,000rad/s, respectively.

Figures 8 and 9 show the bode plots of the closed-loop TF of the control loops, which show that the closed loop voltage controller provides unity gain for frequencies less than 35Hz. This voltage controller functions as a low pass filter to remove the 60Hz voltage ripple. In addition, for frequencies less than 16.3kHz, the current control controller acts as a low pass filter, rejecting current ripples reflected at the switching frequency.

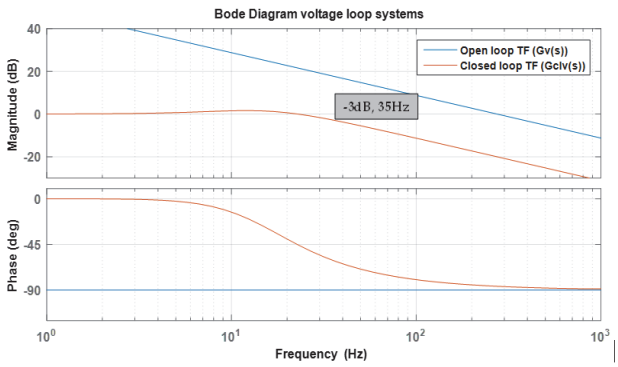


Fig. 8 Bode plot of the PFC stage voltage control system

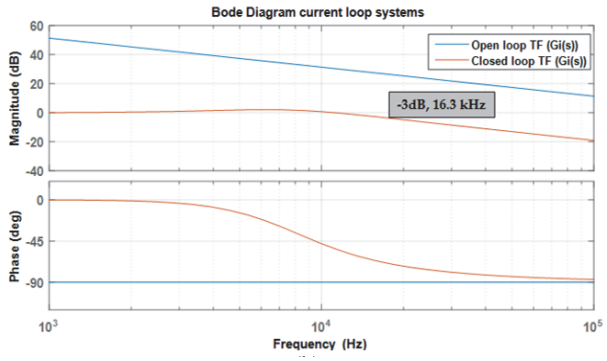


Fig. 9 Bode plot of the PFC stage current control system

3. VSI with LC Filter Stage

The schematic circuit of a full-bridge voltage source inverter (VSI) with an output LC filter is shown in Figure 10, and the design of the LC filter components and the control circuit of the full-bridge switches are presented in the following subsections.

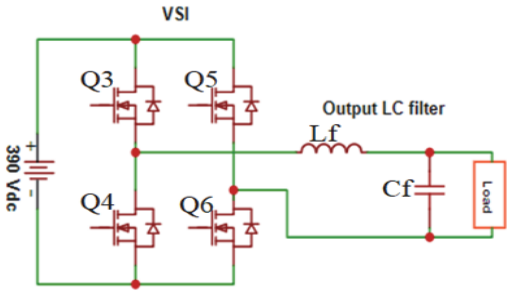


Fig. 10 Schematic circuit of the VSI with LC filter

Switches Q_3 and Q_4 operate at high frequencies, while switches Q_5 and Q_6 operate at low frequencies, resulting in uni-polar modulation. Table 2 lists the switching states used on this reference design. Ascertain that the PWM waveform is symmetric around the zero crossing of the AC wave.

Table 2. VSI stage full bridge PWM sequence

Mode	Cycle	Q3	Q4	Q5	Q6	Vinv
1	+Ve half cycle	on	off	off	on	Vbus
2	+Ve half cycle	off	on	off	on	0
3	-Ve half cycle	off	on	on	off	-Vbus
4	-Ve half cycle	on	off	on	off	0

3.1 Design of the Output LC Filter

The filter inductance is intended to control the current ripple on the VSI's output load side. To determine the optimal value of the filter inductance, the modulation index at the maximum ripple current is calculated. The inductor ripple current is expressed as:

$$V_{bus} - V_{Load} = L_f \times \frac{\triangle i_{Lfrpp}}{D \times T_s} \tag{22}$$

$$\triangle i_{Lfrpp} = \frac{D \times T_s \times (V_{bus} - V_{Load})}{L_f} \tag{23}$$

The duty cycle is calculated using the modulation index (m_i) of the VSI as:

$$D(\omega t) = m_i \times \sin\omega t \tag{24}$$

It is safe to presume that the inverter's output will match the AC voltage:

$$V_{Load} = V_{bus} \times D \tag{25}$$

With substituting from (26), (27) in (25), the inductor ripple current can be re-written as:

$$\triangle i_{Lfrpp} = \frac{V_{bus} \times m_i \times \sin\omega t \ \times T_s \times (1 - m_i \times \sin\omega t \ )}{L_f} \quad (26)$$

Differentiate (26) with respect to time and equate to zero to obtain the modulation index where the largest ripple is present. The modulation index can then be represented as:

$$\sin\omega t = \frac{1}{2m_i} \quad (27)$$

The modulation index for which the ripple is greatest is then substituted back into (23). The required filter inductance value to control the ripple is determined as (28).

$$L_f = \frac{V_{bus}}{4 \times F_{sw} \times \triangle i_{Lfrpp}} \quad (28)$$

The cutoff frequency is kept at Fsw/10 or below to ensure good switching frequency attenuation; hence, the filter capacitance is determined by the fact that the output inductor and capacitor generate a low pass filter that filters out the switching frequency.

$$F_{cut} = \frac{1}{2 \times \pi \times \sqrt{L_f C_f}} = \frac{F_{sw}}{10} \quad (29)$$

$$C_f = \left(\frac{10}{2 \times \pi \times F_{sw}} \right)^2 \times \frac{1}{L_f} \quad (30)$$

Using the voltage source inverter (VSI) parameters given in Table 3, the required filter inductance, and filter capacitance for the VSI stage can be obtained.

Table 3. Design specifications of the VSI stage

Design Specifications		
Parameter	Value	Unit
Input voltage (Vbus)	390 (320-410)	V
Load Frequency (FLoad)	60	Hz
Load Voltage (VLoad)	220	V
Rated load	500	VA
Desired Efficiency (η)	95%	-
Switching Frequency (Fsw)	20	kHz
Current ripple	20%	
Filter cut off frequency	2	kHz

3.2 VSI with LC filter small signal modeling

The equivalent circuit of the studied VSI with an output LC filter is shown in Fig. 11, where the load voltage (V_{Load}) equals the capacitor filter voltage (V_{Cf}). The load is represented as an RL load with a Z_{Load}=R+JWL impedance.

Equations describing the change in inductor current and capacitor voltage of the VSI inverter depicted in Fig. 11 can be written as (31), (32).

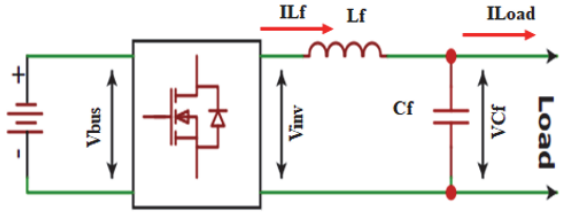


Fig. 11 Circuit diagram of the VSI inverter with LC filter

$$L_f \frac{di_{Lf}}{dt} = V_{inv} - V_{Cf} \quad (31)$$

$$C_f \frac{dv_{Cf}}{dt} = I_{Lf} - I_{Load} \quad (32)$$

The small-signal stability model of the employed VSI with LC filter can be expressed using the same procedure and technique as the average small signal stability modeling used in the PFC converter stage as (33).

$$\begin{bmatrix} \dot{i}_{Lf} \\ \dot{v}_{Cf} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_f} \\ \frac{1}{C_f} & \frac{1}{Z_{Load} C_f} \end{bmatrix} \begin{bmatrix} i_{Lf}^* \\ v_{Cf}^* \end{bmatrix} + \begin{bmatrix} \frac{1}{L_f} \\ 0 \end{bmatrix} V_{inv} \quad (33)$$

3.3 Control Circuits Design of the VSI Stage

Figure 12 depicts the control circuit of the designed VSI with LC filter, which includes the control loops for the load (filter capacitor) voltage and the filter inductor current. The performance of both loops is controlled by PI controllers designed with voltage and current transfer functions obtained from the VSI's small-signal model and the Ziegler Nichols tuning technique for closed-loop control systems.

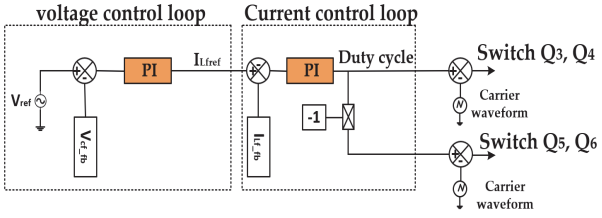


Fig. 12 The structure of the control system for VSI Stage

Using the small signal model obtained in (33), the transfer functions (TF) of the filter capacitor voltage and filter inductor

current systems for the VSI can be expressed as (34), (35).

$$G_{vCf}(s)=\frac{v_{Cf}^{*}(s)}{i_{Lf}^{*}(s)}=\frac{Z_{load}}{Z_{load}\ C_f\ s-1} \tag{34}$$

$$G_{iLf}(s)=\frac{i_{Lf}^{*}(s)}{dinv^{*}(s)}\cong\frac{V_{bus}}{s\ L_f} \tag{35}$$

where the load is represented as RL load with impedance Z_{Load}= R+sL in the s-domin.

Figure 13 shows the block diagrams of the VSI stage's closed-loop voltage and current control loops. The Ziegler Nichols tuning method for closed-loop systems with step input and sustained oscillation at the output is used to obtain the parameters of the PI controllers in both control loops.

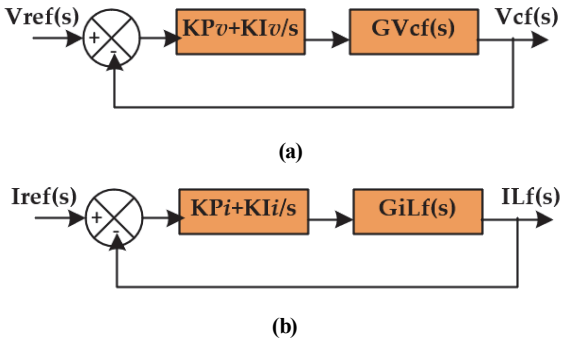


Fig. 13 Block diagrams of the VSI closed loop control systems: (a) voltage loop; (b) current loop

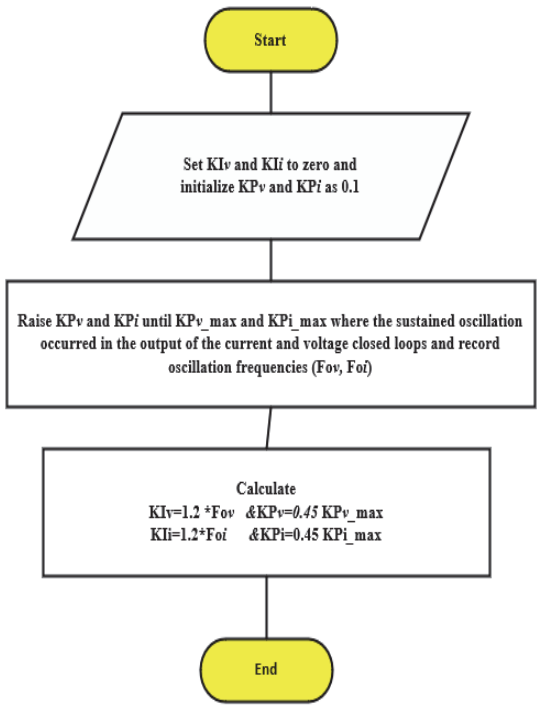


Fig. 14 Ziegler Nichols PI tuning technique

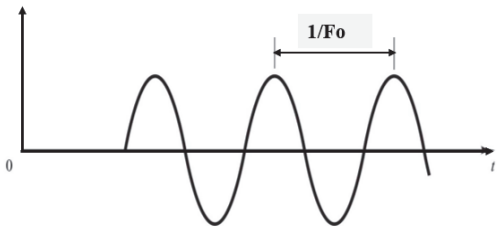


Fig. 15 Closed loop Ziegler Nichols sustained oscillation

Figure 14 depicts the flowchart of the Ziegler Nichols tuning technique used to calculate the PI controller parameters for both control loops. Figure 15 depicts the sustained oscillation of the Ziegler Nichols tuning method during which the controller parameters are calculated.

Table 4 shows the maximum proportional gains, frequency at sustained oscillation, and calculated KP, KI parameters for the voltage and current control loops of the VSI stage using the Ziegler Nichols tuning technique.

Table 4. VSI controllers parameters values

Voltage loop	KP_{v_Max} = 2.20
	F_{ov} = 275Hz
	KP_v = 1 ;KI_v = 334
Current loop	KP_{i_Max} = 1.80
	F_{oi} = 6667Hz
	KP_i = 0.8 ;KI_i = 8000

4. Simulation Results and Discussion

PSIM simulation software is used to test the performance of the proposed AC-AC power supply with the designed power components shown in Table 5 and the designed voltage and current control loops for the PFC and the VSI stages.

Table 5. Designed Power component values

Component	Value	Unit
Boost indictors (L_1, L_2)	240	uH
Bulk capacitor (C_{bulk})	100	uF
Filter inductance (L_f)	3	mH
Filter capacitor (C_f)	20	uF

The EMI filter of the PFC stage is implemented as a CLC filter with a common-mode inductor of 100uH and 1nF capacitors as shown in Fig. 2.

The waveforms of voltages, currents, and power factor of the proposed two-stage power supply are simulated using the same inductive loading condition (R=78ohm, L=0.2H) and varying

input supply voltages from minimum to maximum voltage. Figure 16 shows the performance with a rated input voltage of 220V RMS, demonstrating that the PFC stage's designed voltage control loop successfully regulated the DC bus voltage to the desired value of 390V, and the PFC stage's designed current control loops successfully maintain the phase difference between the supply voltage and current waveforms at about 8 degrees, providing supply with an input PF of 99.05% under inductive loading conditions with a PF of 72%.

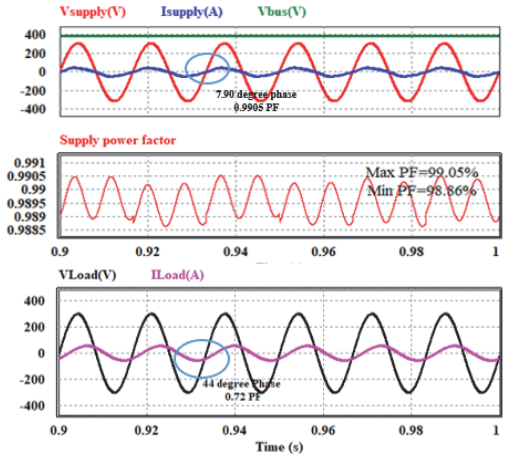


Fig. 16 Voltages, currents, and PF waveforms with rated input supply voltage (220V RMS)

Figure 17 shows the proposed power supply performance at 260V RMS maximum input supply voltage. it can be observed that, the DC bus voltage is also regulated at 390V and the load voltage is constant at 220V RMS when the input voltage is at its maximum. Also, with the same inductive loading condition and PF of 72%, increasing the supply voltage from 220V to around 260V reduces the supply PF from 99.05% to around 97.70%.

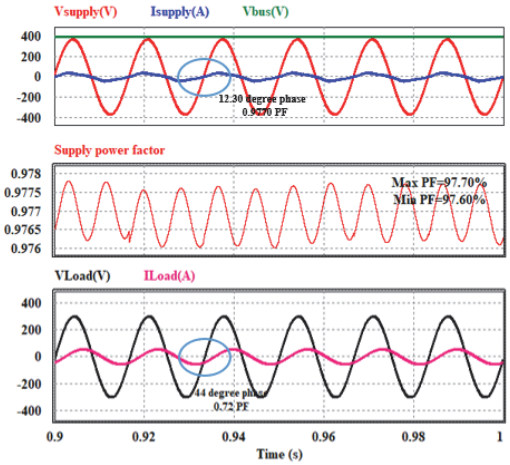


Fig. 17 Voltages, currents, and PF waveforms with maximum input supply voltage (260V RMS)

Figure 18 depicts the proposed power supply performance when the input supply voltage is set to 180V RMS, demonstrating that the DC bus voltage is also regulated at 390V and the load voltage is constant at 220V RMS with a minimum input voltage. In addition, with the minimum supply voltage condition, the supply input PF increases to approximately 99.58%.

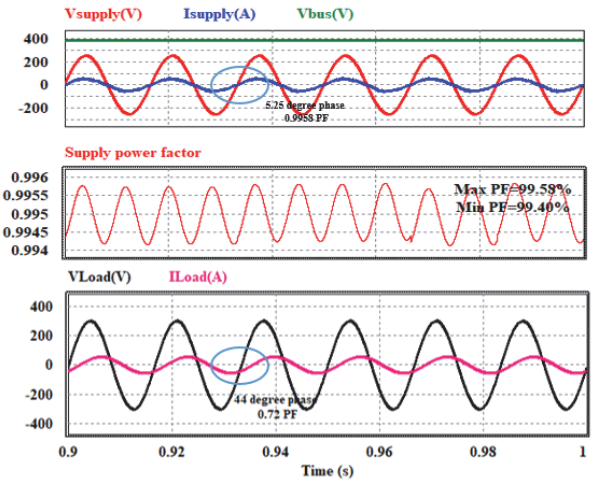


Fig. 18 Voltages, currents, and PF waveforms with minimum input supply voltage (180V RMS)

With the rated supply voltage of 220V RMS and with different inductance loading conditions, the supply PF, load PF and the power efficiency of the designed two-stage power supply are measured and depicted as shown in Fig. 19, which shows that with loading condition with PF of (60-80)%, the supply power factor is more than 99% and the power conversion efficiency is more than 90%.

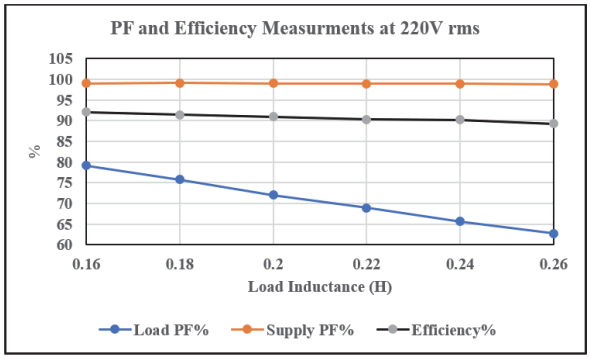


Fig. 19 PF and efficiency measurements with different loading condition

The supply currents THD contents are determined and depicted in Fig. 20 under various inductance loading situations and different supply voltage conditions. With supply voltages of 180V and 220V, the designed power supply provides input

supply current with a THD of less than 10% under loading conditions with PF ranging from 60% to 80%. With a 60% PF load condition, the THD content in the supply current increases to about 15% when the specified power supply operates at the maximum supply voltage limit of 260V RMS.

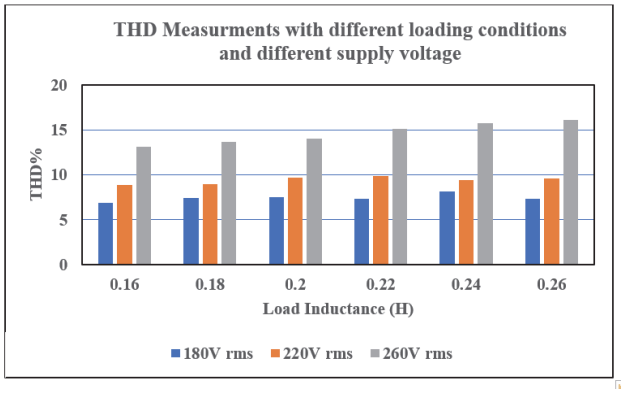


Fig. 20 Supply current THD measurements with different loading condition and different supply voltage

5. Conclusion

This paper proposes a two-stage AC-AC power supply consisting of a PFC converter and a VSI with an LC filter circuit that is suitable for supplying power to inductive loads with a high input power factor, low THD, and high efficiency. The proposed power supply two-stage small-signal models are derived based on average small-signal stability modeling, and based on the derived models, the voltage and current control loops of the power supply PFC and VSI stages are optimally designed to maintain the supply PF at the highest value and regulate the DC bus voltage and load voltage at the desired values with different loading conditions and different input supply voltages, as shown in the simulations. The two-stage power supply with a wide input voltage range from 180V to about 260V RMS and 99% PF for the inductive industrial loads is achieved in this work.

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